特集 Impact of SiC Structural Defects on the Degradation Phenomenon of Bipolar SiC Devices*

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In-house developed (1$\bar{1}$00) and (11$\bar{2}$0) oriented 4H-SiC wafers, and a reference wafer were used to evaluate the impact of the SiC structural defects on the degradation phenomenon of bipolar pn diodes. Evaluation of the crystal quality and the degraded devices was performed by comparing the results of etch pit densities, electroluminescence, Berg-Barrett topography, HRXRD and HRTEM analysis. Our data demonstrate that the degradation phenomenon is strongly related to the SiC structural crystal defects of the starting material. DENSO (HQ) wafers are less susceptible to the forward current degradation, which we attributed to comparatively much lower etch pit densities, specially the slip/stacking fault defects.

Key words : Bipolar pn diode, Degradation, Stacking faults, Carrier recombination, Berg-Barrett topography, HRXRD, Electroluminescence, HRTEM

1. INTRODUCTION

SiC technologies for the manufacturing of power devices seem to be promising in the near future. Today, the commercially available SiC devices, MESFETs and SBDs are manufactured by Cree and Infineon technologies, respectively. In the field of unipolar switching devices, the current trends are the Accu-MOSFET/ECFET[1] and JFET[2] structures, which exhibit the best specific on-resistance experimentally obtained so far. Bipolar power devices stand to benefit greatly in high voltage and high temperature applications. However, the reliability of bipolar devices are hampered by the structural defects. It has been shown that pn diodes exhibit a drift in the forward voltage after the extended forward operations[3]. The degraded bipolar devices showed development of stacking faults in the basal plane extending through the entire epilayer and were attributed to the recombination-enhanced movement of dislocations. In this work, we investigated the impact of SiC structural defects on the degradation phenomenon of bipolar pn diodes fabricated on in-house developed high quality 4H-SiC wafers.

2. EXPERIMENTAL

To investigate the forward current degradation in the bipolar devices, 600V class pn diodes were fabricated in 10μm n-type epi-layers grown on n^+ wafers. Two type of in-house developed 4H-SiC DENSO (HQ), DENSO (STD) wafers, and a reference wafer were used to evaluate the impact of the SiC structural defects. The p-type anode, floating ring edge termination and n-type field stopper EQR were sequentially implanted with Al and P dopants, respectively to achieve a planar pn device structure. Mesh type anode metallization was used to observe the electroluminescence (EL) across the device under the forward bias conditions. The anode active area is about $1.6\times10^{-3}cm^2$. Fabricated pn diodes were stress tested at current densities of about $200A/cm^2$ and $600A/cm^2$. The EL images were acquired using the image intensifier module and a CCD camera (Hamamatsu image intensifier module V7233A). The Berg-Barrett geometry was employed for the reflection X-ray topography using CuKα radiation. The g vector used for the topography was <11$\bar{2}$8>. The incident angle was about 20.5deg. and the absorption depth is about 18μm for (11$\bar{2}$0) oriented wafers. The HRXRD evaluations were performed using a double axis diffractometer with a four reflections Ge (220) crystal monochromator (Phillips X'Pert MRD). The atomic structure of degraded devices were investigated by cross-sectional HRTEM. The TEM samples were

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prepared using precision low angle ion-milling and examined in Hitachi UHV-H9000 top-entry HRTEM with an information limit in the range of 0.16-0.18nm, operating at 300kV.

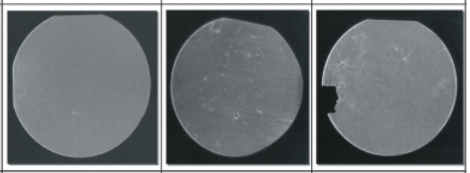
3. RESULTS AND DISCUSSION

Table 1 shows the measured etch pit densities (EPD) of three type of 4H-SiC wafers used in the present forward current degradation analysis. Micro-pipe and screw dislocations affect the off-state characteristics of power devices. Edge dislocations and slip/stacking faults deteriorate the on-state performances in bipolar operations. It should be noted that the EPD, specially the slip/stacking faults of in-house developed DENSO (HQ) wafer is about 1-2 order of magnitude lower than that of other wafers. **Table 2** shows the summary of the Berg-Barrett topography results and the HRXRD extracted parameters. The X-ray topograph of DENSO (HQ) wafer reflect the high crystal quality. The crystal bending was estimated along the off-axis direction by ω-rocking curves. No measurable crystal bending was recorded for the DENSO (HQ) wafers. On the other hand, the crystal bending was found to be convex and concave for DENSO (STD) and reference 4H-SiC wafers, respectively. In addition, the observed record ω-scam FWHM alue of 7-8 arcsec endorse the high quality of DENSO(HQ) wafers as shown in **Fig. 1**.

Table 1 Measured etch pit densities of 4H-SiC wafers (ø15mm size) used in the present investigations
DENSO (HQ) and DENSO (STD) stand for the in-house developed high quality and standard wafers, respectively.

4H-SiC Wafers / Defect Type	DENSO HQ (11$\bar{2}$0) off 8deg.	DENSO STD (1$\bar{1}$00) off 8deg.	Reference (11$\bar{2}$0) off 8deg.
Etch pit density [cm^{-2}]	**8.0×10^{3}**	**1.6×10^{5}**	**3.2×10^{4}**
(i) Micro-pipe density [cm^{-2}]	0	30	15
(ii) Screw dislocations [cm^{-2}]	2.9×10^{2}	2.7×10^{4}	6.7×10^{2}
(iii) Edge dislocations [cm^{-2}]	7.3×10^{3}	1.1×10^{5}	1.6×10^{4}
(iv) Slip/stacking faults [cm^{-2}]	3.8×10^{2}	2.5×10^{4}	1.6×10^{4}

Table 2 Summary of Berg-Barrett topography and HRXRD extracted parameters

4H-SiC wafers	DENSO HQ (11$\bar{2}$0) off-oriented	DENSO STD (1$\bar{1}$00) off-oriented	Reference (11$\bar{2}$0) off-oriented
Berg-Barrett topographs			
Curvature type	-	Convex	Concave
Radius [m]	>3000	9.3	11.5
FWHM [arcsec]	8	11.2	14.9

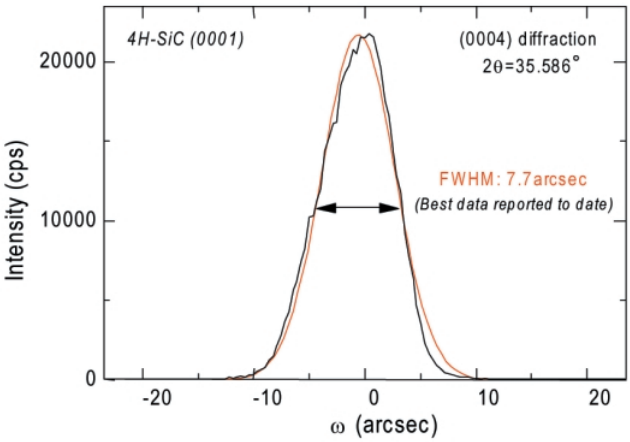


Fig. 1 HRXRD ω-rocking curve of high quality of DENSO (HQ) wafers

The forward characteristics of bipolar pn junction diode fabricated on DENSO HQ 4H-SiC wafers is shown in **Fig. 2**. The blue-violet EL from the pn diode can be observed directly by the naked eye when the devices are forward biased at elevated current densities. The observed EL results from near-bandgap transitions of free carriers and from free-to-bound recombination of free carriers on shallow dopants. EL images of pn diodes before and after the forward current stress at current densities of about 200A/cm^2 and 600A/cm^2 are shown in **Fig. 3**. The images (a) and (b) were acquired using the image intensifier module and a CCD camera at the current densities of 10μA/cm^2 and 600A/cm^2, respectively. EL observation reveals the formation of triangular type structural defects after the forward current stress . The bright lines observed at low current densities were formed as a result of high current density stress effect. These bright lines are viewed as dark features at high current densities and are

attributed to a localized reduction of carrier lifetime caused by the creation of extended stacking faults. The defect grows in the direction perpendicular to the off-axis direction. The nucleation and propagation velocity of defect seems to be different, depending on the quality of the 4H-SiC wafers. We observed that the defect generation rate is relatively higher for pn junction diodes fabricated on wafer with higher EPD values. These defects degrade the device performance by causing a drift in the forward voltage under extended forward conduction. Forward characteristics of degraded pn junction diode fabricated on reference wafer in log and linear scale are shown in **Fig. 4**. The created extended stacking faults degrade the pn junction performance due to large recombination current as ivident from the forward characteristics. The created stacking fault also causes a drift in the forward voltage (ΔV=1.5V@600A/cm^2).

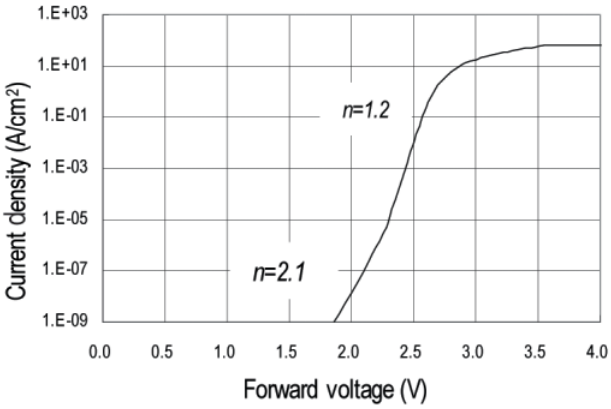


Fig. 2 Forward characteristics of pn junction diode fabricated on the DENSO HQ 4H-SiC wafers

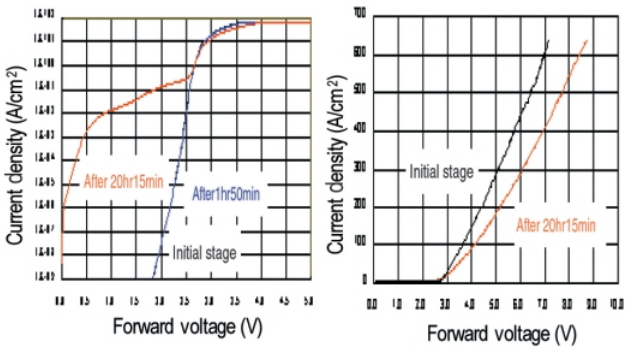


Fig. 4 (a) Forward characteristics degraded pn diode fabricated on reference wafer in (a) log, and (b) linear scale

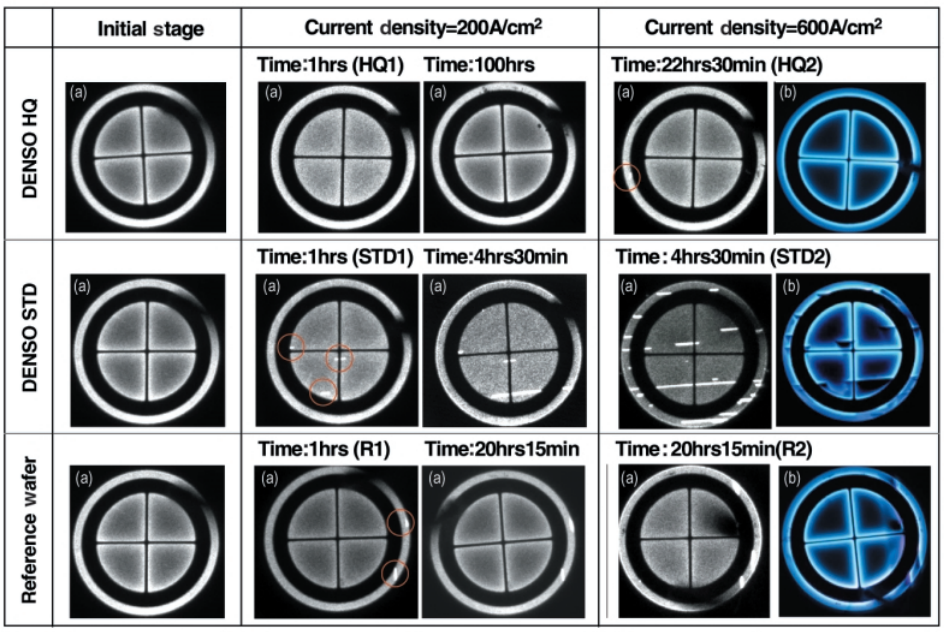


Fig. 3 EL images of pn diodes before and after the forward current stress at current densities of about 200A/cm^2 and 600A/cm^2
The images (a) and (b) were acquired using the image intensifier module and a CCD camera at the current densities of 10μA/cm^2 and 600A/cm^2, respectively.

The DENSO (HQ) wafers are less susceptible to the forward current degradation, compare to other wafers considered in this work. **Fig. 5**. shows a low magnification cross-sectional TEM image of a degraded pn diode fabricated on 4H-SiC DENSO (STD) wafer. From EL observations, it was observed that the multiple stacking faults were nucleated only after the stress test. It seems that the stacking fault nucleate near the implanted region/epilayer interface and move towards the epilayer/wafer interface. As evident from **Fig. 5**, the TEM observations support the EL results. The high resolution TEM image of the generated stacking fault edge in [11$\bar{2}$0] projection is shown in **Fig. 6**. The position of the stacking fault edge is marked by an arrow in the figure. In 4H-SiC polytype, three type of stacking faults configurations are possible,[4] viz., (i) Intrinsic Frank fault; Zhdanov ś notation (3,0), (ii) Extrinsic Frank faults; (4,1), and (iii) Shockley fault (3,1). Our HRTEM data suggests the stacking fault structure as the single layer Shockley type fault bounded by partial dislocations with Burgers vector of a/3<1$\bar{1}$00> type. The a/3[1100] slip must be required to make such a stacking sequence ABCBABCBABCB,,, → ABCBACACBCAC,,, as observed in **Fig. 6**. Shockley faults are created by shear stress, therefore, it may be possible that the observed stacking fault is the result of recombination enhanced plastic deformation of the pn diode. The usual mode of plastic deformation of SiC is the glide of basal plane perfect dislocations with Burgers vector a/3<11$\bar{2}$0>. At low temperatures, deformation occurs by motion of partial dislocations which produces macroscopic stacking faults.[5) 6)] The built-in stress in the pn diode structure may drives the deformation process, while the electron-hole pair recombination provides the necessary activation energy for the motion of partial dislocations. The mechanism responsible for the formation of Shockley type stacking fault needs further clarification.

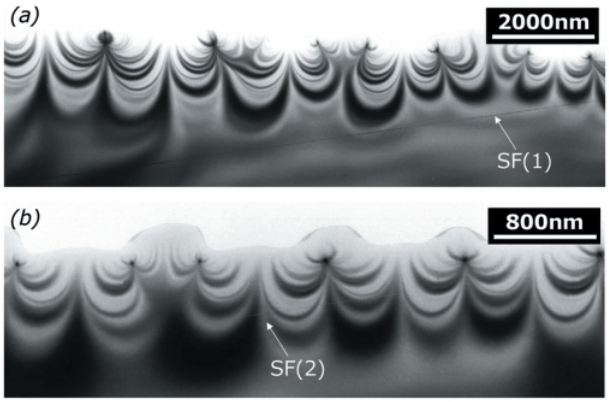


Fig. 5 Cross-sectional images of degraded pn diodes fabricated on DENSO (STD) wafers
(a) Marked straight line corresponds to the stacking fault (SF1) nucleated near the implanted region/epilayer interface, and
(b) Another stacking fault (SF2) terminated in the drift epilayer region

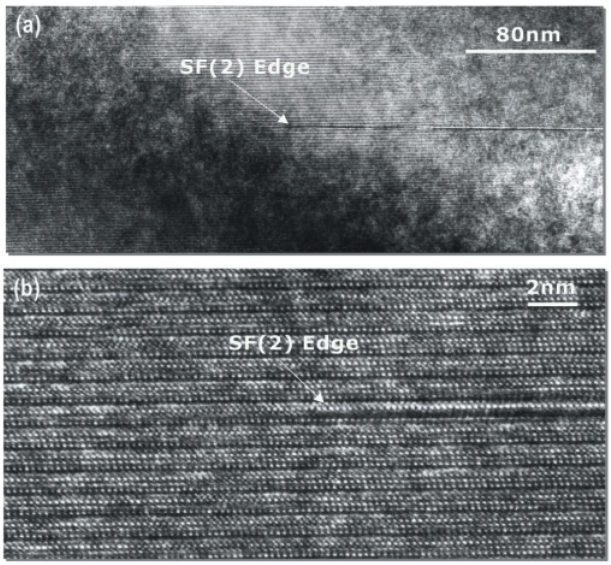


Fig. 6 Cross-sectional images of degraded pn diodes fabricated on 4H-SiC DENSO (STD) wafers (a) Low magnification, and (b) High magnification TEM images of stacking fault (SF2) edge in the drift epilayer region

4. SUMMARY

We presented the impact of SiC structural defects on the degradation phenomenon of bipolar pn diodes. (1$\bar{1}$00) and (11$\bar{2}$0) off oriented 4H-SiC wafers were used to evaluate the pn diode forward current degradation phenomenon. The pn diodes were fabricated under

identical processing conditions. It was demonstrated that the degradation phenomenon is strongly related to the SiC structural crystal defects of the starting material. In-house developed DENSO (HQ) wafers are less susceptible to the forward current degradation, which we attributed to comparatively much lower EPD values, specially the slip/stacking fault defects. Observed record ω-scam FWHM value of 7-8 arcsec endorse the high quality of the DENSO (HQ) wafers. The continuous SiC material development will eventually lead to the robust bipolar device in the future.

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