特集 An All-Digital A/D Converter with 12 μV/LSB Using Moving-Average Filtering*

渡辺高元　水野　保　牧野泰明
Takamoto WATANABE　Tamotsu MIZUNO　Yasuaki MAKINO

A compact, high-resolution A/D converter (ADC) especially for sensors is presented. The basic structure is a completely digital circuit including a ring-delay-line with delay units (DUs), along with a frequency counter, latch and encoder. The operating principles are, firstly, the delay time of the DU is modulated by the A/D conversion voltage; secondly, the delay pulse passes through a number of DUs within a sampling (= integration) time, and the number of DUs through which the delay pulse passes is output as conversion data. Compact size and high resolution were realized with an ADC having a circuit area of 0.45mm² (0.8 μm CMOS) and a resolution of 12 μV (10kS/s). Its non-linearity is ±0.1% FS per 200mV span (1.8−2.0V), for 14 bit resolution. Sample holds are unnecessary, and a low-pass filter function removes high-frequency noise simultaneously with A/D conversion. Thus, the combination of this ADC and a digital filer that follows can eliminate an analog prefiler to prevent the aliasing before A/D conversion. Also both this ADC can be shrunk and operated at low voltage, so it is an ideal means to lower the cost and power consumption. Drift errors can be easily compensated by digital processing.

Key words : A/D converter, ADC, Analog-digital conversion, Sensor interface, High-resolution, Moving-average, Filter, CMOS, Digital integrated circuits, Low power, Low voltage, Delay line, TDC.

1. INTRODUCTION

Advanced systems (automobiles, medical and other electronic devices) have come to use multiple sensors in recent years, and the number is expected to increase even more in the future. The basic structure of the sensors (pressure, accelerometer, yaw-rate, rotation speed etc.) includes a sensing element (hereinafter "element"), and electronic circuits. Since the signal level is generally very near zero, on the order of tens of millivolts, these weak signals must be amplified several hundred times by an analog circuit. On the other hand, user requirements for sensors have become more and more demanding, including the need for high performance and lower cost.

Therefore, there are four major problems in predicting the analog type sensors of the near future. The first issue, from an economic perspective, is the difficulty of shrinkage due to loss of accuracy. The second problem involves greater sophistication of, for example, self-correction and self-diagnostics. The third issue is environmental durability. The fourth problem relates to improving reliability.

Research on digitalization of sensor circuits has become energized as efforts are made to resolve these problems.[1)−5)] To realize digital sensing, the weak signal from the element must be A/D converted at an early stage within the sensor chip, so an ADC is required which has a high resolution of several hundred μV or less. The main reason for applying ΔΣ-ADC in research is its unique high resolution.[1) 3) 5)−10)] However, it requires an analog integration circuit. Thus, a new ADC for sensors is needed.

In the present paper we first discuss, in the next section, the applied concept and the architecture of the new ADC, and prototype evaluation results in section 3. The efficacy of this technology is discussed in section 4, together with examples of applications.

2. THE NEW ADC ARCHITECTURE

2.1 Principles of operation

We conceived a unique A/D conversion architecture involving digitization of the number of stages of a delay unit (DU) in a delay-line through which a pulse passes within a specific time as a novel method which does not have any passive elements such as resistors or capacitors. The principle is illustrated in **Fig. 1**. **Figure 1**(a) shows the pulse delay circuit serially connected to the DU consisting of two nearly minimum-size

inverters, shown in **Fig. 1**(b), wherein the delay time (***Td***) of the DU is modulated by the voltage Vin for A/D conversion. In this way the ***Td*** is changed with high sensitivity.

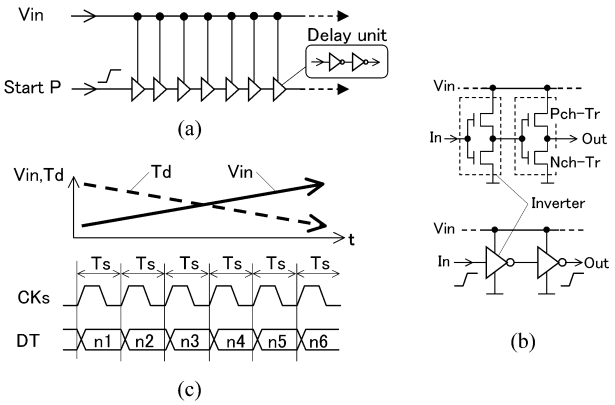

Fig. 1 Principle of operation: (a) Circuit construction (b) Delay unit DU (c) Concept of operation

Figure 1(c) briefly shows the operation of reducing the ***Td*** as the input voltage ***V***in increases. **Figure 1**(c) also shows a digital value (DT) reflecting the input voltage ***V***in that can be obtained by digitizing the number of DUs through which the pulse passes during a fixed time ***Ts***, and output as output data DT. If current sub-micrometer CMOS technology is used, the ***Td*** is extremely fast at approximately 1 ns. For example, when the sampling time (***Ts***) = 10 μs, the number of delay stages of the DU is approximately 10,000, and A/D conversion data equivalent to 10 bits are obtained simply by modulating the ***Td*** by merely 10%. Since the number of stages of the delay pulse passing through the DU is dependent on the ***Ts***, the A/D conversion resolution is controllable by setting the ***Ts***. Operation with this method will always be 10—100 times faster (or with higher resolution) than either traditional voltage-to-frequency converter (VFC) type or current-to-frequency converter type sensing circuits,[11)−13)] if realized with same process technology.

2.2 Basic circuit structure

Generally, 10—14 bits are necessary for a sensor ADC, and the required DU has at least 20,000—200,000 stages. In order to reduce the size of the circuit, a structure has been considered which uses a ring-delay-line (RDL) as the delay circuit to determine the frequency of the delay pulse,[14)] as shown in **Fig. 2**. This new structure actually provides 16 stages of the DU (which means an even number (2^5) of inverters),[15)] and since the frequency counter is 14 bits, it is equivalent to a delay unit having a maximum of 18 bits (262,144 stages).

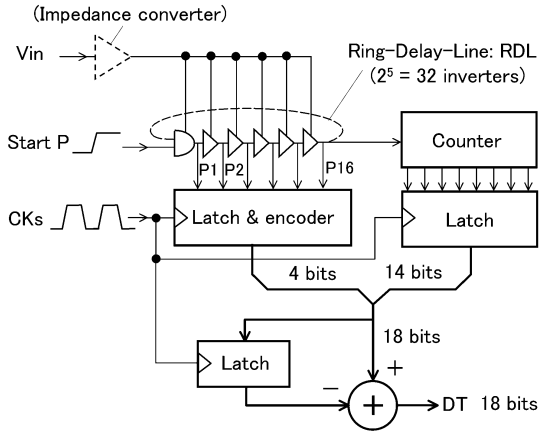

Fig. 2 Block diagram of the A/D converter (TAD)

Since there are a few delay units, the area voltage-modulated by the input voltage ***V***in can be extremely small so as to match well the mutual characteristics of the DUs. Finally, an original architecture for the ADC was made possible by applying a circuit system[14)−16)] devised to allow stable reading of the frequency of an RDL operating at high speed. This ADC system is not only very small, but also has a very wide dynamic range. Data on the difference between successive data from the latches are output as conversion data. In addition, it is not a problem to use an input impedance converter (broken-lined buffer in **Fig. 2**), when the element output format is not proper for direct input of the ADC Vin (see section 5).

This new ADC digitizes extremely short times when viewed from the perspective of direct operation. According to this definition, the new ADC system can be called a time A/D converter (TAD).[17)] Incidentally, TAD can also be used as time-to-digital converter (TDC) ICs as in 18), 19) and 20), by keeping Vin constant for the supply voltage of the RDL.

2.3 Filter effect

In general, the sensor requires a low-pass filter (LPF). We present our new low-pass filter system using no resistor and no capacitor, only a delay circuit. When the *V*in includes high-frequency noise, microscopically, the pulse in a delay time is shortened/lengthened by the noise in the RDL. However, the effect of the A/D conversion is to output a digital value reflecting the average voltage during the *Ts*. Since the TAD operating principle is to obtain the moving average of the voltage change within the *Ts* period, a low-pass filtering effect is generated simultaneously with A/D conversion. This effect is called the TAD filter.

Although traditional dual slope ADCs[21)−23)] have the same concept of filtering, it is impossible to remove resistors, capacitors and analog op-amps. In addition, the TAD operating speed is at least 100−1,000 times faster than traditional dual slope ADCs.

3. SAMPLE EVALUATION RESULTS

3.1 Experimental results of A/D conversion

The TAD prototype IC was fabricated by the 0.8μm CMOS. The TAD circuit area is 0.9mm by 0.5mm. A/D conversion characteristics at a sampling frequency *fs* = 10 kHz (25℃) are shown in **Fig. 3**(a) (evaluation device: analog/digital tester model T7341; Advantest Corp.; input voltage step = 5mV). Approximately 40,000 −260,000 digital values correspond to voltage change in an A/D conversion range of 1.65−5.00V. For example, 55,000−72,000 digital values correspond to an input voltage span of 200mV in a range from 1.8 to 2.0V set as the sensor application range, with the change component being 17,000. Accordingly, the voltage resolution (*Vd*) is extremely high (14 bits) at approximately 12μV/LSB. Non-linearity is ±0.1% FS per 200 mV, and does not pose a problem for sensor application (incidentally ±5.0% FS per 2.0−5.0V span for 18 bit resolution). Voltage resolution increases and integral non-linear error decreases particularly on the

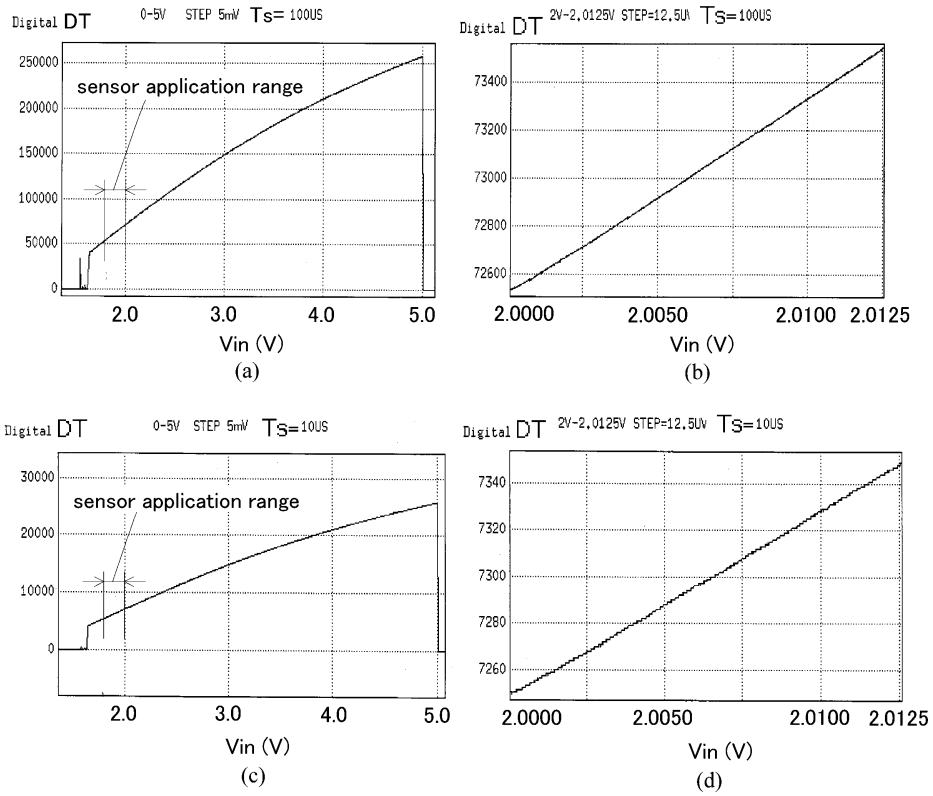

Fig. 3 Characteristics of A/D conversion:
(a) Vin range 1.65−5.00V at a sampling frequency = 10 kHz (b) Partial enlargement of (a)
(c) Vin range 1.65−5.00V at a sampling frequency = 100 kHz (d) Partial enlargement of (c)

low voltage side overriding the triode region of transistors. Time resolution (Td) of the DU in this range is approximately 1.4—1.8ns. This time resolution Td is approximated by the following equation (1)[24] :

$$Td = A\,V\mathrm{in} / (V\mathrm{in} - V\mathrm{th}) \;:\; \alpha = 1.4 - 1.6 \qquad (1)$$

where A and α are constant depending on process technology. **Figure 3**(b) is a partial enlargement (input voltage step: 12.5 μV). Fluctuation was ±3 LSB in the total evaluation system.

Next, A/D conversion characteristics at a sampling frequency fs = 100 kHz (25℃) are shown in **Fig. 3**(c). For example, in the same range of sensor application, the voltage resolution (Vd) is also high (11 bits) at approximately 120 μV/LSB. **Figure 3**(d) is a partial enlargement (input voltage step: 12.5 μV). Fluctuation was ±1/2 LSB in the total evaluation system. In addition, **Figure 4** shows the dispersion of the resolution Vd; that is, the differential voltage ΔV between the code-to-code variation (ΔV = [V in(min) at code: M+1]—[V in(min) at code: M]) with noise (including RDL jitter, bias line and ground line noise) at the sampling frequency fs = 100 kHz (25℃) (where M is ADC output data). The voltage resolution Vd average is 118.6 μV/LSB, and the σ of the distribution is 19.4 μV for the Vin range 1.800—1.824 V (total data counts = 206). **Table 1** shows TAD performance characteristics (with 1 MS/s results).

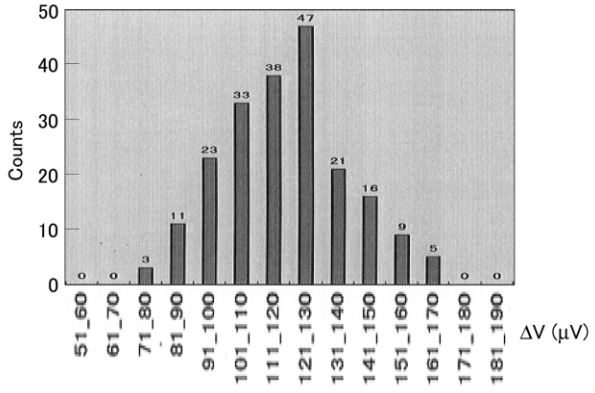

Fig. 4 Histogram of the dispersion of the resolution Vd; that is, the differential voltage ΔV between the code-to-code variation with noise (including RDL jitter, bias line and ground line noise) at a sampling frequency = 100 kHz

Table 1 Summary of ADC (TAD) characteristics

Parameter	fs = 10 kHz	fs = 100 kHz	fs = 1 MHz
sampling rate	100 μs	10 μs	1 μs
resolution	12 μV/LSB	120 μV/LSB	1.2 mV/LSB
input voltage span	200 mV	200 mV	200 mV
number of bits	14	11	7
non-linearity	±0.1 % FS		
power	< 1 mW (VDD = 2 V)		
active area	0.45 mm² (0.8 μm CMOS)		

Incidentally, resolution density drift was approximately (-20%, +40%) relative to 25℃ in a range of -35—140℃,[17] but can be resolved by digital calculation correction to obtain the ratio to a reference value.[17] This concept is the same as in the "dual slope" method.[21)—23)] Although resolution may be somewhat imprecise at high temperatures, since TAD does not require an analog circuit, it is applicable to high temperature sensors because of its stable operation at a high temperature of 140℃.[17] Since the correction calculation may be accomplished by joint use of the signal processor employed for element characteristic correction in time division, or using a correction program executed by microcomputer, additional circuits are unnecessary. In addition, it may be that servo-controlled sensors do not need to compensate the drift errors of TAD resolution.

3.2 Experimental result of TAD filter

The TAD filter effect is shown in **Fig. 5**. The solid line shows the plot of the amplitude characteristic of the theory of moving average for continuous signals by the following equation at the sampling frequency fs = 100 kHz.

$$u(\tau, t) = \frac{1}{\tau}\int_{t}^{t+\tau} \sin 2\pi f v dv \qquad (2)$$

In this equation, τ is the sampling time Ts (10 μs), and the dots indicate experimental results of TAD output data. The plot of the TAD characteristic completely fits the theory of moving average effect.

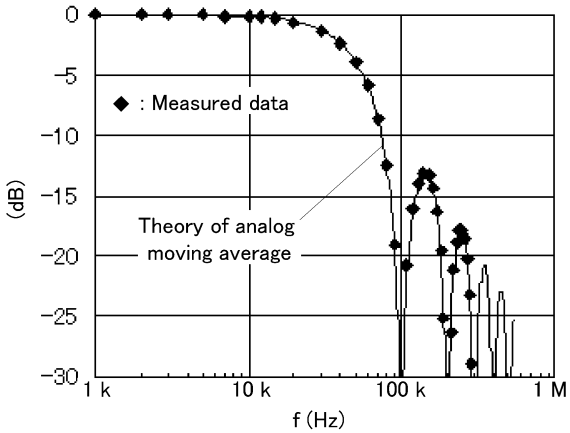

Fig. 5 TAD filter evaluation result at a sampling frequency = 100 kHz

4. DISCUSSION

4.1 Programmable ADC sensitivity

The TAD can improve actual signal amplification by increasing *Ts*. The number of stages through which the pulse passes in the DU is increased by increasing the *Ts*, with the result that conversion data of great amplitude are obtainable. A high degree of *Ts* reproducibility is required (minimal clock jitter), but does not pose a problem insofar as a typical quartz resonator clock is used. Conversely, when low sensitivity is desired, the *Ts* may be easily reduced.

4.2 TAD filter effect eliminating prefilter

The TAD differs from conventional A/D converters in that it basically does not require a sample hold because erroneous operation does not occur even with random voltage fluctuation during A/D conversion. Specifically, by determining the RDL frequency, the accuracy of the mean processing is increased. In addition, for more sophisticated mean processing it is very important that the delay characteristics of the 16 individual DUs in the RDL are mutually uniform.

One of the advantages of TAD is that an analog prefilter is unnecessary to prevent the aliasing generally required before A/D conversion, because the TAD filter can remove high-frequency noise which passes through the digital filter (arrows in **Fig. 6**(b)). Additionally, the digital filer that follows TAD can eliminate components of the aliasing with A/D conversion by TAD. **Figure 6** shows the simulation results of (a) TAD filter characteristics, (b) digital filter characteristics averaging 10 data and (c) combination TAD filter and digital filter, at a sampling frequency of 100 kHz. In this case the aliasing level is less than −25 dB. Generally, elements ' signal bandwidth is less than 10kHz. In addition, for wideband inputs, the oversampling technique can be applied because TAD operates relatively fast at more than 1 MS/s, although it reduces ADC bits (**Table 1**). If the ADC bits must be maintained, making a TAD parallel construction is effective.

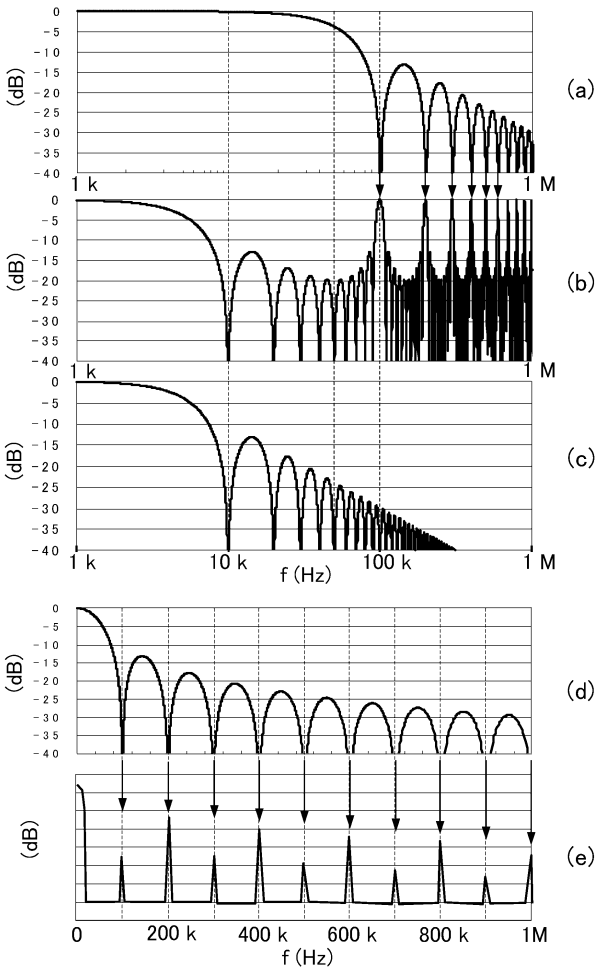

Fig. 6 Simulation results:
(a) TAD filter
(b) Digital filter (averaging 10 data)
(c) Combination TAD filter and digital filter (averaging 10 data)
(d) TAD filter
(e) Image of components of A/D conversion signal with clock-noise (sampling frequency = 100 kHz)

4.3 TAD filter effect removing clock-noise components

Another advantage of the TAD filter is that it removes highly effectively the high-frequency noise due to operating clocks using discrete-time analog circuit techniques, such as synchronous detection and switched-capacitor (SC). **Figure 6**(d), (e) briefly shows the clock-noise reducing effect by applying the periodically appearing notch parts of a TAD filter (**Fig. 6**(d)). By using the same clock or a clock divided by N (N: integer) as a TAD sampling clock, the notch part frequencies, that is, the infinite attenuation regions, completely fit the component frequencies of the operating clock, as shown in **Fig. 6**(e) by arrows, which exist as components of an A/D conversion signal with clock-noise.

5. SENSOR IC PROTOTYPE

An IC test chip (0.65 μm CMOS) of a digital sensor integrating TAD and correction processing circuits is shown in **Fig. 7**. Signals from each type element are externally input. In this figure the small frame has the TAD and the large frame the digital correction processor automatically designed by the automatic layout system. TAD is simply shrunk from a 0.8 μm CMOS. In this IC, first the detection signal Vin and reference signal Vr (built in the IC) are quickly A/D converted alternatively by TAD, and the data ratio (Vin/Vr) is then calculated by the digital correction processor (this concept is the same as in the "dual slope" method[21)–23)]), after which a digital averaging process is executed. This chip is capable of detecting weak input signals with extremely high reproducibility (precision: 10 μV). A low-frequency noise reducing effect is realized by calculating (Vin/Vr) because TAD has an extremely wide dynamic range and the signals (Vin as numerator, Vr as denominator) have the same noise level.[25)] With this method, the degradation in the quality of detecting signals that is caused by the input impedance converter (as shown in **Fig. 2**) can be avoided. In this IC we need to do that (calculating (Vin/Vr)) often enough to cancel drift errors due to temperature, supply voltage and other drift factors. A CR resonator clock built into the CMOS chip is used as the sampling clock source.

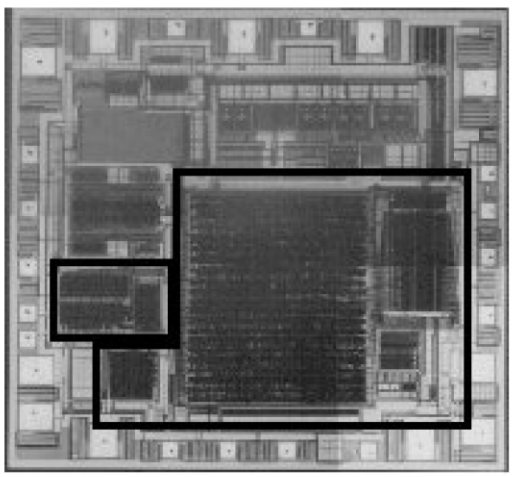

Fig. 7 Sensor test chip with TAD (small framed area) and digital correction processing circuits (large framed area)

This sensor IC operates with the same level of precision as a bipolar IC using a standard CMOS.[26)] This example is actual proof that high-accuracy signal processing is possible using inexpensive CMOS technology. New possibilities also arise in the application of CMOS technology to realize 1-chip smart sensors.

6. CONCLUSION

In the expectation of the future digitalization of sensors, we have implemented an original ADC architecture (TAD) via a completely digital circuit for use as an A/D converter in a sensor. The TAD is compact, shrinkable and capable of high resolution. Using a prototype IC, we experimentally confirmed a 14-bit dynamic range with a resolution of 12 μV/LSB. TAD is capable of eliminating high-frequency noise simultaneously with A/D conversion via the TAD filter effect. Highly accurate signal detection was verified in an IC prototype of a digital sensor with integrated TAD and correction processing circuits (reproducibility precision: 10 μV). Therefore, implementation of micro sensors combining TAD and microelements can be expected. Digital sensor circuits using TAD have a high environmental durability comparable to typical digital circuits. Hereafter, we intend to pursue applications in

various types of sensors. Advances in process technology and parallel A/D processing of multiple TADs will enable faster and faster sampling rates. It should also be mentioned that TADs may well be able to replace some kinds of conventional ADCs in days to come.

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<著　者>

渡辺　高元
（わたなべ　たかもと）
第２開発部
センサ回路，デジタルIC関連の機能回路技術研究開発に従事

水野　保
（みずの　たもつ）
第２開発部
センサ回路，デジタルIC関連の機能回路技術研究開発に従事

牧野　泰明
（まきの　やすあき）
IC技術２部
半導体センサ回路関連の技術開発に従事