論文 Normally-off Accumulation-mode Epi-channel Field Effect Transistor*

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Silicon carbide (SiC) is an attractive wide band gap material for robust high power electronics because of its exceptional electrical and physical properties. MOS based SiC power devices are being developed to replace the Si for high temperature and high power applications. This paper provides an overview of the normally-off accumulation-mode epi-channel field effect transistor (ECFET) design concept that is particularly applicable to SiC. The challenges for power device development beginning from wafer quality to key device process of thermal oxidation are discussed. Finally, the applicability of these ideal switches in hybrid electric vehicle (HEV) propulsion inverter system is reviewed.

Key words : SiC, MOSFET, Accumulation-mode ECFET, MOS interface, Thermal oxidation, Interface defects

1. INTRODUCTION

The MOSFETs have been one of the most versatile devices in Si and is the building block for most VLSI application. SiC MOSFET can revolutionize the high voltage switching applications in the blocking voltage (V_B) < 5.0kV. For such a high voltage range, typically Si power devices utilize conductivity modulation in the drift region to reduce the forward drop, however, compromising with the switching speed of the device. SiC power devices has the capability for high temperature operations in the range ~200˚C for MOS based and ~400˚C or higher for non-MOS based devices. Today about 15% of the electric power produced undergoes some form of electronic conversion that mostly occurs at the consumer end. Therefore, there is strong demand for the improvement of the following critical parameters of the power inverter systems viz., (i) Cost (low device and circuit cost, modularity), (ii) Size (weight, volume, and foot-print), (iii) Efficiency (low conduction and switching losses, fast switching capabilities), and (iv) Reliability (rugged high temperature operations, high blocking stability, and low random failure).

SiC is unique among compound semiconductors in that its native oxide is SiO_2, the same oxide as Si. The GaN and AlGaN have high breakdown field and high carrier mobility, and would appear to be ideally suited for power device implementation. However, these III-V nitride compounds do not possess a native oxide similar to SiO_2, so true MOS devices will not be feasible. In addition, the nitrides suffer from the lack of a suitable lattice-matched substrate for crystal growth, and hence these materials are in a more primitive state of development than SiC. Various figure-of merit were calculated in order to quantify the advantage of SiC over the Si viz., Johnsons Figure-of-Merit, Keys Figure-of-Merit, and Baliga Figure-of-Merit. The Baliga Figure-of-Merit (BFM) is for power devices in general defined by Baliga in 1989.[1] BFM ($V_B^2/A\ R_{ON}$) is a single quantity that represents how closely the device approaches the theoretical limits for the semiconductor material. The theoretical maximum BFM for Si unipolar devices is about 5 MW/cm^2, whereas the theoretical limit for 4H-SiC unipolar device like MOSFET is about 2000 MW/cm^2. Compared to bipolar Si-IGBTs, considerable reduction in static and dynamic losses can be achieved for the unipolar power MOSFETs. However, the inversion-mode 4H-SiC MOSFET performance is still hampered by the problem of low channel mobilities due to the high interface trap density near the conduction band edge (D_{NIT}). Refined oxidation techniques have improved the SiO_2/SiC MOS interface quality, but producing reliable devices still require a process innovation. Recently, there has been significant progress in producing high power devices for power and high frequency applications.[2][3] From the HEV application point of view, inverter system power module require high-efficiency, high-functionality, and high-reliability.[4][5] Existing HEV inverter systems use Si-IGBT based power modules. Being a unipolar switching device, SiC MOSFETs are the ideal replacement for Si-IGBTs. This paper provides an overview of the normally-off accumulation-mode ECFET design concept and the challenges for SiC power device development. In addition, the applicability of these ideal SiC switches in HEV propulsion application is also reviewed.

2. DESIGN OF SiC POWER MOSFETs

Until DENSO's trench 4H-SiC ECFET reported in ICSCRM'97,[6][7] SiC power MOSFETs had not significantly exceeded the Si theoretical limits. ECFET is basically an accumulation-mode MOSFET in which a thin n-type epi-channel layer was grown on the p-type base region to form an accumulation-mode power device. The use of an accumulation-mode channel improved the MOSFET channel mobility significantly, resulting in the lowest specific on-resistance (R_{ON}) of about 10.9mΩcm^2 at room temperature with controlled avalanche breakdown voltage (V_B) of about 450V, the first Si-limit breaking performance by any SiC power switching device. Although, there exists a trade-off between the R_{ON} and V_B, however, since then the SiC MOS based power device design is evolving mainly on the accumulation-mode MOSFET design concept in efforts to utilize the maximum potentials of SiC material.

2.1 Accumulation-mode SiC ECFET

The main feature of ECFET is that the n-type channel-forming region is epitaxially grown on the p-base region to form the MOS structure. This epi-layer provides an independent control of the impurity concentration of the channel and the p-base region. Therefore, a power MOSFET with high blocking voltage, low specific on-state resistance and low threshold voltage can be designed such as to allow independent control of the dopant concentration

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of the different regions. Since, the concentration in the p-base region can be raised independently, therefore, the thickness of the p-base region can be reduced. This helps in trimming the JFET component of R_{ON}, compared to the inversion-mode structure. Moreover, in the accumulation-mode conduction, the channel depth is about 5~10x larger than that of the inversion-mode channel, thereby the current conduction is less affected by the MOS interface conditions. The accumulation-mode channel mobility is expected to be higher than the inversion-mode channel mobility due to relaxation of electric field. The epitaxially grown n-type epi-layer that define the channel region can be completely depleted by the potentials created by the work function difference between the p-base region and the epi-channel layer, and the work function difference between the epi-channel layer and the poly-Si gate electrode. ECFET can be turned-on by applying the positive bias to the gate electrode. This design concept can withstand up to the avalanche breakdown conditions. We reported the fabrication of first accumulation-mode trench 4H-SiC ECFET on (000-1) plane 4H-SiC epi-wafers.[6)7)] On the similar accumulation-mode channel design, a blocking voltage of about 1.4kV was reported for the 4H-SiC IOP-ACCUFET.[8)] IOP effectively eliminated oxide breakdown in the trench corner, allowing the device to reach 87% of the theoretical value. The R_{ON} was 15.7mΩcm² with Figure-of-Merit of 125 MW/cm², a value 25x higher than the theoretical limit for Si-MOSFET. In trench MOSFET design, practically it's difficult to realize the high blocking voltages due to the poor gate oxide reliability, as the electric field is higher near the bottom of the trench corners.

Chilukuri et al.[9)] reported the fabrication of planar accumulation-mode MOSFET, called ACCUFET on (0001) plane 6H-SiC n-type epi-wafers. Accumulation-mode mobility as high as 120cm²/V.s was reported for the fabricated device. However, they reported the problem related to the p-type dopant boron (B) diffusion from the p-base region. Usually, high power applications require a high level of unit-cell integration, which can be achieved by reducing the pitch of unit-cell. The B diffusion can limit the reduction of p-base spacing due to increasing JFET pinch resistance. We reported a novel C/B sequential implantation process to control the B lateral and vertical diffusion from the p-base region of the planar ECFET.[10)] The schematic cross-section structure of our proposed accumulation-mode planar ECFET is shown in **Fig. 1**. The B vertical and lateral diffusion as shown in figure can lead to serious design problems and electrical performance degradation of fabricated device. The B lateral diffusion into the JFET region results in high on-state resistance or even completely blocks the current conduction due to pinch effect phenomenon. We performed the 2D numerical device simulations using ISE DESIS simulator to access effect of B lateral diffusion on the ECFET on-state characteristics. Three ECFET models with different B lateral diffusion length were considered viz., diffusion length=0μm (without diffusion), 0.5μm, and 1μm. The B lateral diffusion simply translates a decrease in the p-base spacing of the ECFET unit-cell. The simulated potential contours for the 26μm unit-cell ECFET with (diffusion length =1μm) and without B lateral diffusion are shown in **Fig. 2**. The contours gradient

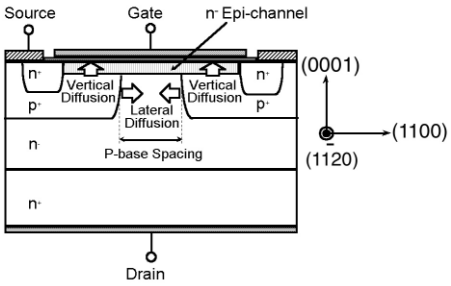

Fig. 1 Schematic cross-sectional structure of accumulation-mode planar ECFET

in the JFET region indicates the voltage drop in that region. The voltage drop is higher in the JFET region for the case where B diffusion was considered. The simulated on-state characteristics of ECFET indicates the strong affect of B diffusion on the R_{ON} due to JFET pinch effect as the drain current is reduced by a factor of 1/3 for lateral diffusion length of 1μm for a given drain and gate bias conditions. Therefore, it is vital to suppress the lateral as well as vertical diffusion of B to fabricate the accumulation-mode ECFET. Aluminum (Al) is another p-type dopant for selective implantation process, however, require the relatively high temperature activation annealing and also yield more residual defects in comparison with B dopant.

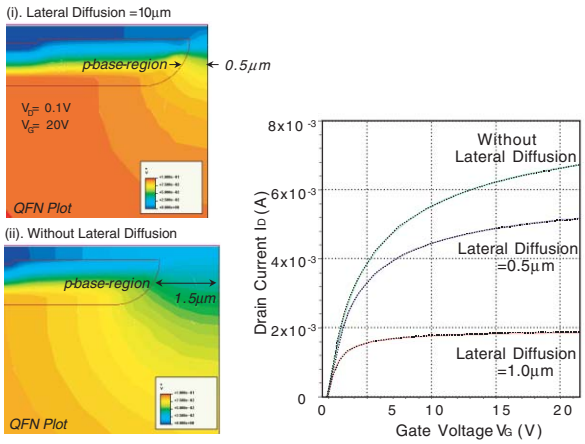

Fig. 2 Simulated potential contours in the planar accumulation-mode ECFET. Simulated output characteristics of ECFET with and without B lateral diffusion are also shown in the figure

The planar ECFET was fabricated using (0001) plane n/n⁺ 4H-SiC epi-wafer. The device fabrication details are given elsewhere.[11)] Typical on-state output characteristics of the fabricated planar ECFET with and without the B lateral diffusion at room temperature are shown in **Fig. 3**. Excellent I_D-V_D characteristics were obtained for the planar ECFET without B lateral diffusion as the device shows good current saturation and gate control. The threshold voltage measured at V_G=V_D was about 2.0V. The effectiveness of C/B sequential implantation process in suppressing the JFET pinch effect is clearly visible from the 3~4 fold increase in drain current of ECFET for p-base spacing which was scaled down to about 3μm. Therefore, this technique opens

door for the larger packing densities through unit-cell pitch reduction for power device applications by suppressing the B diffusion to match the design requirements. The fabricated device features the controlled avalanche V_B of about 1.2kV.

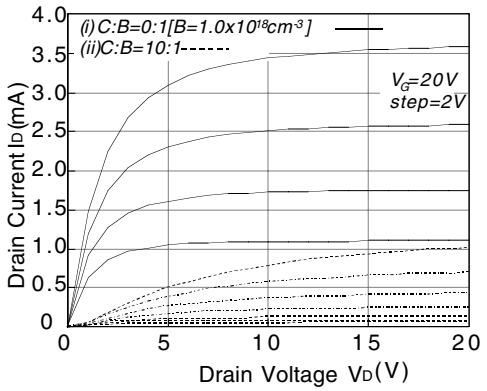

Fig. 3 Typical on-state output characteristics of the fabricated planar 4H-SiC ECFET with (i) B implanted and (ii) C/B sequentially implanted p-base region

The 1st SiC trench MOSFET was reported by Cree Inc. in 1993[12] and the 1st accumulation-mode SiC ECFET with R_{ON} lower than that of Si-limits was reported by DENSO CORPORATION in 1997.[6] The V_B as high as 5.0kV for SEMOSFET has been reported by KEPCO and Cree.[13] The R_{ON} was 88mΩcm² with Figure-of-Merit of 284MW/cm², a value about 50x higher than the theoretical limit for Si-MOSFET. The power MOSFETs reported to date[14)15)] indicates that although the V_B has increased steadily over the past 10 years, there has been slow reduction in R_{ON}. This is because the specific on-resistance of 4H-SiC MOSFETs is still dominated by the channel resistance, rather than by the drift region resistance. The relatively high channel resistance is due to relatively low channel mobility, particularly in the 4H-SiC polytype. The reduction of channel resistance is vital for any further improvement in the performance of MOS based SiC power devices. For an insight of the future trends of SiC power devices, relations between blocking voltage and specific on-resistance of conventional unipolar and super junction devices is shown in **Fig. 4**. The specific on-resistance of conventional SiC power devices will be trimmed further by one or two order of magnitude, depending on the targeted blocking voltage using the RESURF technology in the future.[16]

Selection of SiC Polytype: Bulk Electron Mobility Anisotropy

4H-SiC polytype is the material of choice for power device applications because of (i) nearly isotropic high bulk electron mobility in comparison to 6H-SiC, (ii) availability of relatively high quality wafer, and (iii) advanced processing technologies including epitaxial growth. Earlier, Schöner et al.[17] had reported a comparison for inversion-mode channel mobility of 4H-, 6H-, and 15R-SiC MOSFETs under the identical processing conditions. They observed low inversion-mode channel mobility for 4H-SiC MOSFETs and

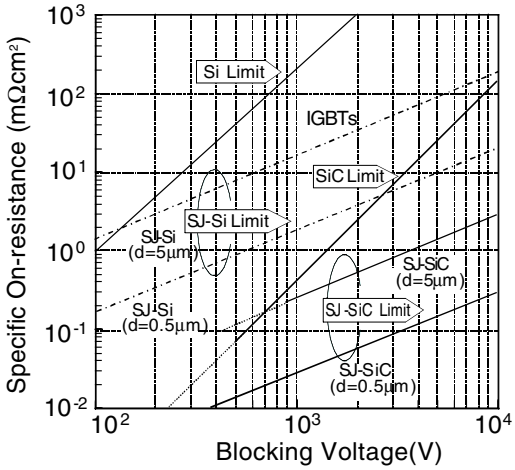

Fig. 4 Specific on-resistance and blocking voltage plot for conventional unipolar and super-junction Si and SiC power devices

attributed it to the high density of interface states located at approximately 2.9eV above the valence band edge or just below the conduction band edge of 4H-SiC. More of these states lie in the band gap for 4H-SiC (E_G=3.3eV) compared to 6H-SiC (E_G=3.0eV) where they affect the channel mobility via carrier trapping and Coulomb scattering. Afanasev et al.[18] originally reported the existence of near interface trap states between the conduction band edge of 4H- and 6H-SiC, which acts as the scattering centers at the MOS interface. They proposed that interface states in SiC/SiO_2 structures result from C-clusters at the interface and defects in a near-interface sub-oxide. 6H-SiC MOSFETs have shown moderate inversion-mode channel mobility, however, the performance of 6H-SiC vertical power MOSFETs are limited by lower bulk mobility in the direction parallel to the c-axis, which is about 1/10 of 4H-SiC. Alternatively, the 15R-SiC is another attractive solution as the band gap of this polytype is smaller than that of 4H-SiC, therefore, the inversion-mode channel mobility is less influenced by near interface trap states. In addition, the bulk mobility of 15R-SiC is less anisotropic in nature. Therefore, 15R-SiC is a promising polytype for power device applications, however, the large size high quality wafers are not yet available.

Selection of Crystal Plane: Channel Mobility Anisotropy

As mentioned earlier, anisotropic nature of the bulk electron mobility is an important parameter for power device design. The channel mobility anisotropy is another important design parameter that determines the device performance. The step controlled epitaxial growth on the conventional (0001) plane requires off-axis 6H-SiC (3.5deg. off) or 4H-SiC (8.0deg. off) substrates to inherit the polytype information from the substrate. The surface roughness introduced by the use of off-axis wafers may affects the MOS interface properties and thereby channel mobility. Yano et al.[19] reported a dramatic improvement in the inversion-mode channel mobility of 6H- and 4H-SiC MOSFETs fabricated on (11-20) plane by using on-axis substrates. The planar SiC MOSFETs on (11-20) plane have also shown the negative temperature dependence of channel mobility that was

observed for the first time. These results indicate that the (11-20) plane may be the best selection for SiC MOSFETs, however, the maximum breakdown electric field in (11-20) plane is only 75% of that for the (0001) plane and that limit the use of this plane for the power MOSFETs with $V_B < 2kV$. The best reported inversion-mode mobility values are typically~50cm²/Vs and~150cm²/Vs for the planar MOSFETs fabricated on (0001) and (11-20) oriented 4H-SiC wafers, respectively,[20] the oxide reliability issues are yet to be addressed.

3. SiC MATERIAL QUALITY AND KEY DEVICE PROCESS TECHNOLOGY

In SiC device fabrication process, various high temperature conflicting processes influence strongly the SiC MOSFETs channel mobility. Fabrication process steps like thermal oxidation, p-type dopant activation, and Ohmic contact annealing collectively degrade the channel mobility. The process dependent channel mobility degradation of SiC MOSFET is still poorly understood to date. The key technological issues include (i) True defect free large size (~4"size) off-axis <0001> oriented and on-axis <11-20> oriented SiC wafers, and (ii) High quality SiO_2/SiC MOS interface process and its high temperature reliability. This is the most critical factor for MOSFET practical applications.

3.1 Quality of 4H-SiC Large Size Wafers

Recently, 600V class SBDs and MESFET are available commercially from Infineon Technologies[2] and Cree Inc.,[3] respectively. Infineon Technologies has announced the market introduction of cascode switching (normally-on SiC-JFET + Si-MOSFET) devices. However, the high quality and large diameter wafer is a prerequisite for industrial-scale fabrication of power devices which to date lacks for SiC. The greatest challenge is the quality of the material, which limit both current capability and yield of such devices with respect to the chip area. Development of SiC wafers has been very successful over the past years in achieving major improvements in quality and yield. However, there are particular areas where SiC wafers are still significantly behind state of the art Si wafers technology viz., (i) SiC wafer size which is currently available in 2" and 3" diameters (research level: 4" diameter), (ii) Lack of high quality material as SiC wafers still contains various type of defects, and (iii) SiC wafer process technology (Warp, TTV, LTV, etc.) is still demanding. The crystal defects such as μ-pipe defect, comet-tail defect, dislocations, and impurities within the active region of large area devices affect both on- and off-state characteristic adversely. At present, the dislocation density in the commercially available wafer is in the range of ~10^4cm^{-2}. The secondary effects of dislocation centers on leakage current or breakdown phenomenon are not clear at present. There are several thermodynamic, kinetic, and technological mechanisms, which causes μ-pipe formation in SiC wafer. The μ-pipe defects generally propagate into the LPCVD grown epitaxial layers, which leads to premature junction breakdown below the maximum permissible electric field. The μ-pipe density of less than 1cm^{-2} is needed to realize devices of current ratings >100A with reasonable yield. Recently, <11-20> oriented SiC wafers are commercially available from Cree. The key epitaxial growth and selective ion-implantation technologies appear very feasible on <11-20> oriented wafers, which indicates that the manufacturing of SiC power devices is promising in the near future.

4H-SiC Wafer Quality Versus Bipolar Forward Degradation

In the HEV inverter power module, 600V class IGBTs are generally used in parallel with and Si-PiN FWD to conduct the reverse current for IGBTs. Bipolar power devices stand to benefit greatly in high voltage and high temperature applications. The MOSFETs can be used as a bi-directional switch and the internal pn body diode can eliminate the needs of the external FWDs. Recently, the bipolar forward degradation phenomenon[21] characterized by an increase of the forward voltage caused by forward operation has been reported. Such an electrical degradation of bipolar pn diode can limit the use of the internal body diode of SiC MOSFETs. The suppression of the bipolar forward degradation is vital for the future development of such an ideal switches.

Earlier, we presented the impact of SiC structural defects on the forward current degradation of pn diodes fabricated on in-house developed high quality 4H-SiC wafers.[22] The pn diodes were fabricated on in-house developed (1-100) off oriented 4H-SiC standard (STD) and (11-20) off oriented 4H-SiC high quality (HQ) to evaluate the impact of SiC structural crystal defects. **Table 1** shows the measured etch pit densities of three types of 4H-SiC wafers used in the present forward current degradation analysis. The etch pit density, especially the slip/stacking faults of DENSO HQ wafer is about 1~2 order of magnitude lower than that of other wafers. These values reflect the high quality of in-house developed 4H-SiC wafers. Moreover, these wafers of size φ15mm are free from the μ-pipe defects. The electro-luminescence (EL) images of pn diodes fabricated on DENSO STD, HQ, and reference 4H-SiC wafers, before and after the forward current degradation are shown in **Fig. 5**. EL reveals the formation of triangular type structural defects after the current degradation. Bright lines observed at low current densities were formed as a result of high current density stress effect. Whereas, these bright lines are viewed as dark features at high current densities and are attributed to a localized reduction of carrier lifetime caused by the creation of extended defects viz., the stacking faults. The propagated defect looks like a single layer Shockley type stacking fault bounded by partial dislocations with Burgers vector of a/3 <1-100> type. These created extended defects degrade the device performance due to large recombination leakage current. The defect grows in the direction perpendicular to the off-axis direction and often grows until it span over the whole device area. The nucleation and propagation velocity of defect seems to be different, depending on the quality of the wafers. We observed that defect generation rate is relatively higher for pn diodes fabricated on 4H-SiC wafer with higher defect densities. It is shown that the in-house developed DENSO HQ 4H-SiC wafer is less susceptible to the forward current degradation, which we attributed to comparatively much lower EPD values. These results demonstrate that the degradation phenomenon of bipolar pn diodes is strongly related to the SiC structural crystal defects of the starting material. The

continuous SiC material development will eventually lead to the robust bipolar device in the future.

Table 1 Measured etch pit densities and HRXRD extracted parameters of 4H-SiC wafers used in the present investigations

4H-SiC / Defect Type	HQ wafer s <11$\bar{2}$0> off 8 deg.	STD wafers <1$\bar{1}$00> off 8 deg.	Reference <11$\bar{2}$0>off 8 deg.
Etch Pit Densities (EPD)	**$8.0x10^3$ cm^{-2}**	**$1.6x10^5$ cm^{-2}**	**$3.2x10^4$ cm^{-2}**
(i) Micro-pipe Density	*$0cm^{-2}$*	*$30cm^{-2}$*	*$15cm^{-2}$*
(ii) Screw Dislocations	*$2.9x10^2cm^{-2}$*	*$2.7x10^4$ cm^{-2}*	*$6.7x10^2$ cm^{-2}*
(iii) Edge Dislocations	*$7.3x10^3cm^{-2}$*	*$1.1x10^5$ cm^{-2}*	*$1.6x10^4$ cm^{-2}*
(iv) Slip/Stacking Faults	*$3.8x10^2cm^{-2}$*	*$2.5x10^4$ cm^{-2}*	*$1.6x10^4$ cm^{-2}*
HRXRD *FWHM [arcsec]*	*8*	*11.2*	*14.9.*
Curvature Type	*Flat*	*Convex*	*Concave*
Radius [m]	*>3000*	*9.3*	*11. 5*

#DENSO (HQ) and DENSO (STD) stand for the in-house developed high quality and standard wafers, respectively.

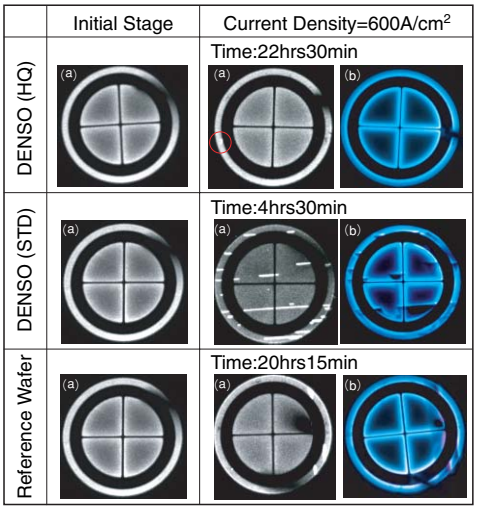

Fig. 5 EL images of pn diodes before and after the forward current stress degradation

3.2 Thermally Oxidized SiO2/SiC MOS Interface

The thermal oxidation kinetics and the MOS interface of SiC are poorly understood as it still lacks the critical know how. Afanasev et al.[18] originally proposed that interface states in SiC/SiO_2 structures result from C-clusters at the interface and defects in a near-interface sub-oxide that is produced when the oxidation process is terminated. The low MOSFET channel mobility might be due to high interface trap density that increases exponentially near the conduction band edge. Relatively one-order higher channel mobility values were reported for 6H- and 15R-SiC MOSFETs, compare to 4H-SiC MOSFET.[17] The microstructure of transient-SiO_2 region in the SiO_2/SiC system is very much different from that of SiO_2/Si system.[23] The C-related compounds such as $Si_4C_{4-x}O_2$ complex and $SiO_{1.5}$sub-oxide interspersed in C-matrix were reported to exist in the transient region. These residual complexes can form clusters or interact with H^+ or OH^- ions under pyrogenic oxidation condition. Therefore, the control over the C in the transient region is vital for improving the quality of MOS interface. Electrical characteristics of MOS interface have shown strong dependence on the pre- and post oxidation conditions. The re-oxidation and O_2-annealing post-oxidation treatments were found to be effective in reducing the C-content near the MOS interface, which was attributed to the reduction of C concentration near or at the MOS interface. The maximum electric breakdown fields above 10MV/cm and interface trap density value below $1x10^{12}eV^{-1}cm^{-2}$ have been reported for thermally grown SiO_2 on (0001) oriented Si-face n-type 4H-SiC.

Earlier, we investigated the interface trap density near the conduction band edge using the thermal admittance (TAS) spectroscopy on 4H-SiC MOS capacitors fabricated under the wet oxidation ambient.[24] N-type 4H-SiC (0001) Si face off-oriented epi-wafers were used in the present investigation. The thickness and nitrogen (N) doping concentration of the epi-layer was 10μm and $1x10^{16}cm^{-3}$, respectively. **Figure 6** shows a series of admittance spectra for 4H-SiC MOS capacitor under various accumulation bias conditions in the range of 0V~15V. The conductance was measured over the temperature range of 80-380K. The admittance spectroscopy can provide the information related to the trap centers in MOS capacitor. It can be seen from the figure that even for 0V bias, tail of peak-A was detected in the measured temperature range that corresponds to the deep traps near the midgap. When the accumulation bias voltage is increased in steps from 0V to 8V, a broad peak was observed for each biasing condition. Under the accumulation condition, the electrons are available near the MOS interface that can be trapped by the interface traps, which are close to the Fermi-level. The admittance signal arises from these charged interface traps. The shift in the peak position towards the lower temperature range indicates lowering of ionization energy or capture cross-section of the corresponding trap states. For 8V bias, two peaks (peak-A and peak-B) appear as a result of response from interface traps of different microstructures. The intensity of the broad peak was also decreased with increasing accumulation bias voltage due to bias effect on the TAS signal. At this point, we think that the D_{NIT} is contributing to the peak-B. Finally, in the strong accumulation region i.e., 15V bias, only peak-B appears which support the above stated statement. The Arrhenius plots of electron emission rate e_pT^{-2} for the trap state calculated from the admittance spectra is shown in **Fig. 7**. The estimated density of traps from the admittance data for peak-A and Peak-B are shown in the Figure.

The ionization energy of broad peak-A shows a strong bias dependence and indicates a broad distribution of these traps below the conduction band down to midgap region. The peak-B corresponds to the traps in the near SiO_2 region and lies very close to the conduction band edge that was first reported by Afanasev et al.[18] The D_{NIT} has strong influence on the channel mobility of 4H-SiC MOSFETs because their ionization energy (ΔE=180meV) lies between the conduction band edge of 4H- and 6H-SiC polytype. However, the D_{NIT} values estimated from the admittance data is in the range of 10^{10}~$10^{11}eV^{-1}cm^{-2}$, which is about 1-order lower values of D_{NIT} that estimated by the capacitance-voltage (C-V) measurements. Bassler et at.[25] also reported the presence of high value of D_{NIT} at 4H-SiC/SiO_2 interface

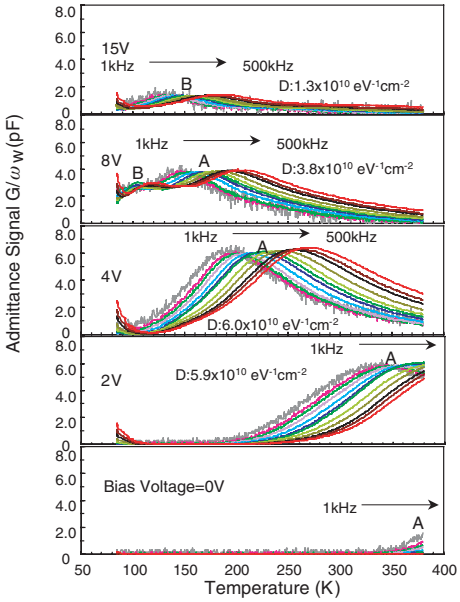

Fig. 6 The admittance spectra for 4H-SiC MOS capacitor under various accumulation bias condition

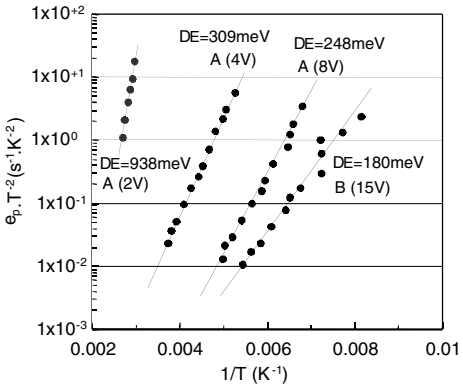

Fig. 7 Arrhenius plots of electron emission rate e_pT^{-2} versus reciprocal temperature

located close to the conduction band edge of MOS capacitors fabricated under the dry oxidation ambient. Novel innovations are needed to bring the D_{NIT} value down to about ~$1x0^{11}eV^{-1}cm^{-2}$ near the conduction band edge.

High Temperature Nitridation Process

Recently, the NO and N_2O annealing at high temperatures has revealed to improve SiO_2/SiC MOS interface properties. The remarkable improvements of the 4H-SiC MOSFET inversion layer mobility were reported using oxide nitridation.[26)-28)] The oxide is usually thermally grown in nitrous oxide atmosphere at 1250˚C. Inversion layer mobility values up to ~50cm²/Vs for lateral 4H-SiC MOSFETs, which were prepared on low doped p-type epilayers and the oxide was thermally grown in nitrous oxide atmosphere at 1250˚C.[29)] This annealing process is considered to have two effects, one is formation of stable Si-N bonds and the other is removal of C-related sub-oxides. However, it is not yet understood which effect brings the improvement of MOS interface properties. Main reason for the improvement should be an increase of channel mobility. The channel mobility increase is may be due to the reduction of the DNIT. The N introduced into the SiO_2/SiC interface can passivate interface states, however, it does not remove the residual-C in the oxide as C was detected by XPS measurements.[30)] Hence, the N itself gives the favorable effect for the improvement of MOS interface properties. The high inversion-mode channel mobility and high temperature reliability using deposited ONO (silicon oxide/silicon nitride/silicon oxide) are also quite encouraging for MOS based devices. The innovations in the SiC oxidation process have improved the SiO_2/SiC MOS interface quality, but producing reliable devices will require additional improvements.

4. APPLICATION OF MOS BASED POWER DEVICES IN HEV INVERTERS

MOS based SiC power switches, with their superior features compared with Si-based switches, can substantially improve the performance of HEV inverter systems. Today's most advanced electric vehicle (EV) still suffers from the insufficiency of the energy storage because of the limited battery capabilities. Compared to fuel tanks, they are inferior in terms of mobility at high costs. The commercial production of HEVs using a combination of electric motors and internal-combustion engines (ICE) for power-train became feasible. HEVs eliminate the limited mobility of electric vehicles. The various technical solutions for hybrid drive systems can be categorized into series and parallel hybrid system. In simplified terms, a series hybrid transfers the power electrically i.e., the electric power produced by an ICE-generator unit is transformed into mechanical power via electric drive motors. The parallel hybrid transfers the power mechanically to the wheels. The power and torque of the ICE and electric motor can be added by running both at the same time. However, the potential to reduce emissions is greater for a series hybrid drive system than of a parallel hybrid. For the inverter of HEV traction motor control system, vital requirements are compactness, lightweight, high efficiency, and high reliability. Existing HEV inverter systems generally use intelligent power modules in an attempt to achieve compact and efficient designs. One of the basic building blocks of power module is the half bridge PWM circuit in which pairs of IGBT switch and anti-parallel PiN FWD are connected in series in a Totem-pole configuration. For the IGBT power module (18-chips in 6-arms) of a rated voltage of 600V and a rated current of 600A, each chip is connected in parallel to each other for each phase arms. The IGBT power module contains within a package the protective functions against over-current, short-circuit, voltage drop, and overheat. Required characteristics for the IGBTs are low losses, high ruggedness, and easy drivability. However, there is a trade-off relation between the power loss and ruggedness. The controller produces gate-driving signal into each phase arms based on the PWM signal from the engine control unit (ECU). The performance of the inverter systems generally depends on the quality of its power chips.

In these IGBT inverters, the circulating current flows through FWDs because these devices can't conduct reversely. In this configuration, when the gate voltage turns the IGBT on, the PiN diode attempts to turn off. The PiN diode drift region is conductivity modulated by minority carrier injection, and there is a substantial minority charge storage that must be removed each time when the diode turns off. Therefore, the transient reverse current in the FWD adds to the motor current flowing through the IGBT, causing the collector current to overshoot. This high current flows while the collector voltage of the IGBT begins to fall, and the IGBT dissipates considerable instantaneous power. Therefore, the turn-on energy loss is given by the integral of the current-voltage product during the overshoot spike. The turn-off losses are mainly dominated by the turn-off characteristics of bipolar Si-IGBT alone. The total switching loss can be roughly classified into two categories: (i) the conduction loss, determined mainly by the product of the voltage and current, when the element is turned-on, and (ii) the switching loss, caused in the transient state of switching. When the carrier frequency reaches or exceeds 10kHz, the switching loss accounts for nearly 50% of all the total inverter loss. The high switching losses lead to high heat dissipation from the power switching devices. Therefore, to increase the efficiency and decrease the cost, weight, and volume of power inverter systems, it is important to reduce this heat dissipation. The higher destruction immunity is required for automobile applications. 600V class (Current rating=200A) planar or trench Si-IGBTs and soft recovery PiN FWDs are being used in the existing inverter systems. FWDs soft recovery characteristics are desired in order to reduce the EMI noise occurring with IGBT switching operations. FWD power loss reduction is particularly important for HEV systems because of the frequent regenerative operations and stall modes. To reduce these switching losses or heat dissipation, both software as well as hardware approaches are available. One of the hardware solutions is to use the unipolar SiC power switching devices. **Figure 8** shows the correlation between the Si and SiC power devices operational frequencies, blocking voltages, temperatures, and the possible applications. Majority carrier devices like the MOSFETs and JFETs offer extremely low switching power losses. Therefore, the application of SiC unipolar devices can drastically reduce both the conduction loss and the switching power dissipation of power inverter systems. The soft switching characteristics also guarantee good EMC behavior. It is expected that SiC MOSFETs will replace the Si-IGBT for the future generation inverter system for medium class power applications in the blocking voltage range <5.0kV. The bipolar devices like IGBTs, and GTOs offer low forward voltage drops at high current densities but have higher switching losses than majority carrier devices. Since a built-in junction potential of SiC is higher than that of Si due to larger band gap, therefore bipolar power devices are attractive with a blocking voltage >5.0kV. There also exists a design trade-off between the switching speed and the on-state voltage drop in a switching power device. In addition, there are other considerations that may be of paramount importance for the circuit designer while making the choice of the switching device for a particular application viz., high temperature capability, radiation hardness, easy current control ability, simple protection under abnormal modes of operation, and operation-mode of device (normally-on or -off type). The high value of thermal conductivity for SiC allows dissipated heat to be readily extracted from the device. This, in turn, allows a corresponding increase in power to be applied to the device for a given junction temperature, while maintaining the power chip destruction immunity. The other advantages of using the SiC MOSFETs is their reverse conduction characteristics and the availability of internal pn body diode that can be used as a FWD to achieve a FWD-less inverter system. The SiC power devices will reduce the conduction losses and the switching losses drastically by 1~2 order of magnitudes depending on the applications. These features allow the construction of power module using fewer power device chips e.g., three Si-IGBT chips in each phase arms can be replaced by a single SiC unipolar MOSFET chip. The FWD-less SiC power module will further helps in the downsizing of inverter system. Cost reduction is one of the most important problems to overcome for the popularization of HEV vehicles. The SiC unipolar power devices have various advantages compared with Si-IGBT, provided the following issues that are limiting the widespread use would find the reasonable solutions. The key issues are (i) SiC wafer size, (ii) low processing yield because of high density of defects, (iii) High cost and limited availability of SiC power devices, and (iv) Unavailability of high-temperature packaging technology.

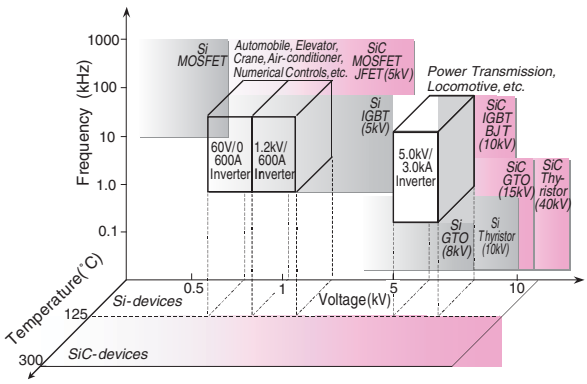

Fig. 8 3D plot showing the correlation between the Si and SiC power devices operational frequencies, blocking voltages, temperatures, and the possible applications

5. CONCLUSIONS

An accumulation-mode SiC ECFET design concept and the key device technologies that face the hard challenges for high power switching applications have been reviewed. The outstanding material issue demands the reduction in the μ-pipe defects and the dislocation density to allow higher yields and larger devices to become practical. We demonstrated that the degradation phenomenon of bipolar devices is strongly related to the SiC structural crystal defects of the starting material. SiO_2/SiC MOS interface fabrication process call for the novel innovations to improve

the MOS interface quality. The interface trap density near the conduction band edge remains high in the range of ~10^{12} $eV^{-1}cm^{-2}$. The D_{NIT} in SiO_2 were observed that severely degrades the channel mobility. The high temperature nitridation techniques have shown reduction in the D_{NIT} values as well as improvement in the MOSFET channel mobility. Finally, the applicability of ideal SiC switches in HEV propulsion application is reviewed. These systems with SiC power devices have the qualities of being more compact, lighter, and efficient.

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