特集 Thermal Cycle Reliability of 3D Chip Stacked Package Using Pb-free Solder Bumps : Parameter Study by FEM Analysis*

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This study seeks to analyze the reliability of three-dimensional (3D) chip stacked packages under cyclic thermal loading. The critical areas of 3D chip stacked packages are defined using Finite Element Modeling (FEM) based simulations to correlate the thermal cycling experiments.

3D chip stacked packages consist of two 300μm thick Si chips vertically connected with Sn-Ag-Cu solder bump joints and then assembled on a conventional FR-4 printed circuit aboard (PCB). Two thermal cycle conditions were studied, namely -40 to 125°C and 0 to 100°C. FEM simulations indicate that in both conditions, the critical failure location is expected to be the chip side region of the corner solder bump of the lower chip connecting the package to the PCB. Creep strain per single thermal cycle averaged over a critical damage volume; $\Delta\varepsilon_{cr}$ was used as the damage parameter.

Furthermore, we have investigated possible approaches to improve the thermo-mechanical reliability of this package. The results indicate that adding an underfill or thinning the Si chips will achieve a lower creep strain in the solder bumps. Furthermore, the stress levels in the Si and Cu via in the Si chip are low. Therefore fracturing of the Si chips and fatigue of the Cu vias is not expected under thermal cycling conditions.

Key words : Thermal cycle, 3D chip stacked package, Pb-free solder, Parameter study, FEM analysis

1. INTRODUCTION

In a three-dimensional (3D) package, semiconductor devices or packages are stacked in the vertical direction. This package is effective in the reduction of a mounting area. Several 3D package concepts[1)2)] have presented in the literature and some types of 3D packages are already in fabrication.

3D chip stacked packages with bumps can more effectively minimize the mounting area on a PCB. Furthermore, by connecting the chips with through via-holes, the resulting reduction in the wiring length allows a faster transmission of the electric signal.[3)4)] Normally, the chips in this package are thin and have many I/Os. This leads to some issues, such as the handling of thin Si wafers during production, bending of devices and a need for improvement of alignment accuracy between devices.

In this study, we have investigated the reliability of the 3D chip stacked package with two Si chips of 300μm thickness and Sn-Ag-Cu solder bump joints (300μm diameter). Furthermore, we have investigated the possibility of increasing the reliability of this package using finite element model FEM (Finite Element Model) simulation.

2. SAMPLE PREPARATIONS

The demonstration device consists of two Si chips connected vertically with Sn-Ag-Cu solder balls. The bottom Si chip has a daisy chain on the lower face in order to allow in-situ four-point measurement of resistance during accelerated temperature cycling test. The chips have 8×8 area array of solder pads with a 1mm pad pitch.

The Si chips are assembled on a FR-4 PCB (printed circuit board) with Sn-Ag-Cu solder balls (**Fig. 1**). The dimensions of the Si chip are 10×10×0.3mm^3 and the diameter of the solder ball is 300μm.

The daisy chain on the bottom chip is formed with plated-Cu circuit and BCB (Benzocyclobutene) is used as a solder mask to restrict the solder pad openings. The thicknesses of both Cu and BCB are 5μm with copper pads of 500μm diameter and 250μm BCB opening. On the other side of chip, a blanket layer of electroplated copper is deposited and BCB openings which mirror the lower side are formed.

The thickness of PCB is 2.5mm. The thicknesses Cu and solder mask on PCB are 50μm, and the diameters of them are 250μm and 300μm, respectively.

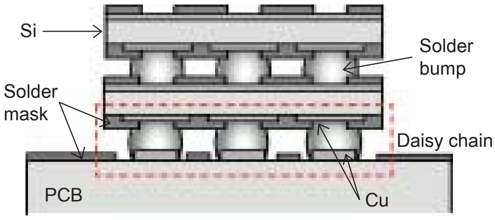

Fig. 1　3D-chip stacked package demonstrator

The reflow profile has a peak temperature of 240°C and the time above liquidus is 60 seconds in an air atmosphere.

After assembly, the quality of the connections is confirmed with X-ray inspection, cross sectioning and the electric resistance measurement of the daisy chain.

3. FEM MODELING

FEM simulations are performed in order to predict a failure mode and as a second stage, to optimize the structure. **Figure 2** shows 3D FE model and close up of the critical bump. Due to the symmetry, only one-eighth of the structure needs to be modeled. All processing; modeling, solving and post-processing tasks are performed using the commercial FE code MSC.MARC.

The material properties used in the model are listed in **Table 1**. Except for Sn-Ag-Cu solder and Cu, all the materials are modeled with isotropic, linear, elastic properties. The equation for the creep strain of Sn-Ag-Cu material is shown below.[5)]

$$d\varepsilon/dt = 2\times10^{21}\sigma^{18}\exp(-9994.59/T)$$

where ε is creep strain, t is time in second, σ is stress in MPa and T is temperature in K. The temperature dependent Young's modulus of Sn-Ag-Cu and the yield stress of Cu are also listed in **Table 1**.

The materials of the structure are assumed to be stress-free at 25°C. Cyclic thermal loads with temperature excursions of -40 to 125°C and 0 to 100°C, at the frequency of 1 cycle per hour are applied.

Furthermore, it is assumed that, the shape of Si chips is perfectly flat before the thermal cycle, although in reality, the Si chips may have some inherent bending induced by the stress from a grinding and thin film deposition.

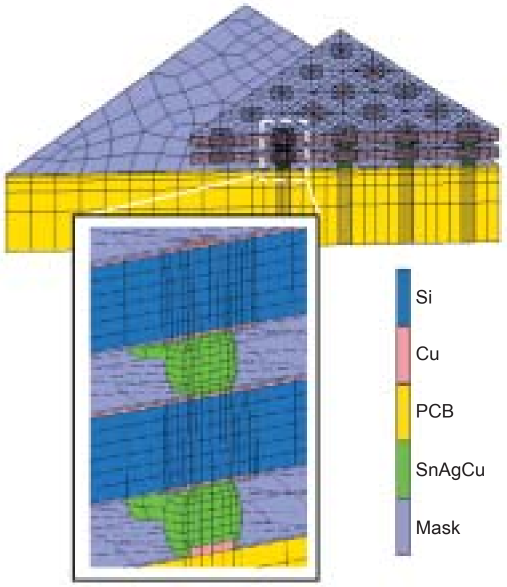

Fig. 2　FEM model for 3D chip stacked package

Table 1　Material properties used in FEM

Material	Young's modulus (MPa)	CTE (10^{-6}/ºC)	Poison's ratio	Yield stress (MPa)
FR-4	19700	17.6	0.3	-
Si	169000	2.3	0.26	-
Solder mask	3000	55	0.3	-
Cu	117000	16.7	0.3	172.3
SnAgCu	52400-193.05T	17.6	0.3	-

4. RESULTS AND DISCUSSION

4.1 3D 300μm-thickness-Si-chip stacked package

Figure 3 shows the view of Si chip with a daisy chain and Sn-Ag-Cu solder balls. The two Si chips are connected vertically as shown in **Fig. 4**. Optical and SEM image analysis indicates a sufficient formation of intermetallic layers to enable a good solder joint formation on both the package and the board side.

In **Fig. 5**, the deformation and the von Mises stress of the 3D chip stacked package during a thermal cycle test (-40 to 125°C) is shown. Due of the mismatch of coefficient of thermal expansion (CTE) between Si and PCB, the solder bumps, especially between 1st Si and PCB (1st bumps) are deformed. On the other hand, the solder joints between 1st Si chip and 2nd chip (2nd bumps) have hardly deformed, because the relative displacement between the 1st and 2nd Si chip is at the same level during the thermal cycle and these

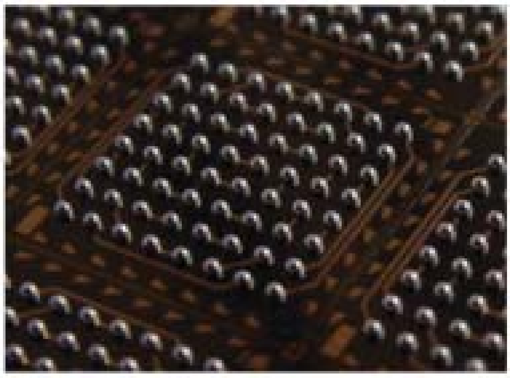

Fig. 3　Top view of Si chips with daisy chain and solder balls

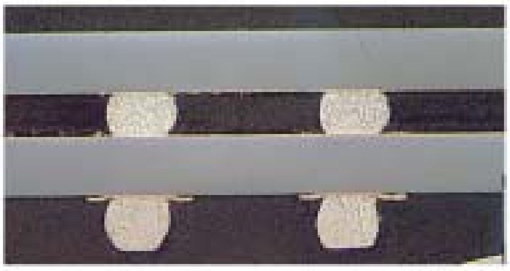

Fig. 4　Cross section of the connected 3D stacked package

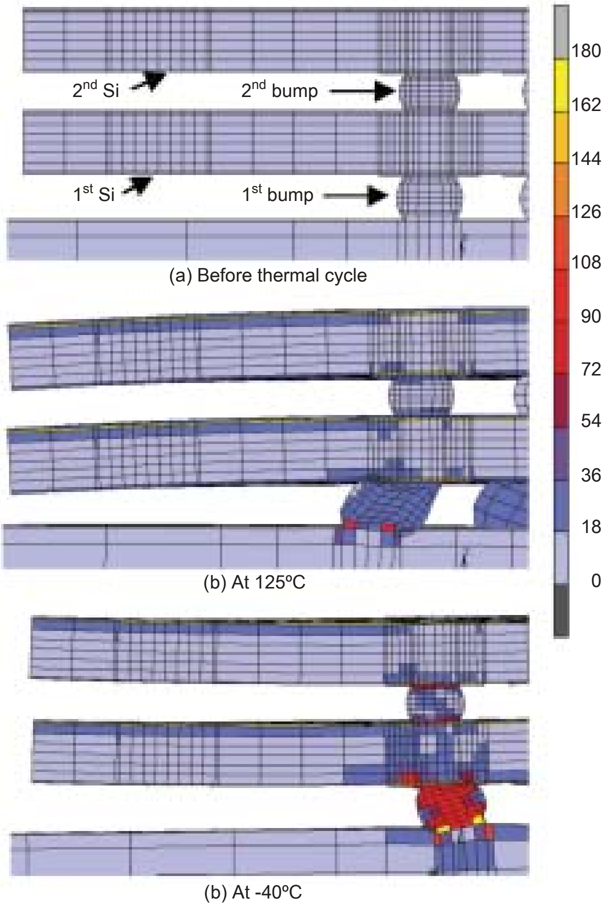

Fig. 5　Deformation and von Mises stress during thermal cycle, -40 to 125 °C (Deformation scale : 40)

solder joints see very little strain imposition.

Figure 6 shows the accumulated creep strain in the critical corner bump on PCB after 3 cycles of -40 to 125°C. It is observed that the maximum creep strain is located in the upper part of the solder joint, close to 1st Si chip. As a damage parameter, we chose $\Delta\varepsilon_{cr}$ (creep strain averaged over a damage volume per one thermal cycle) in 3rd cycle. For the calculation of $\Delta\varepsilon_{cr}$, a damage volume of three (upper part) or two layers (bottom part) of elements, as shown in **Fig. 6**, are selected.

In **Table 2**, the results of $\Delta\varepsilon_{cr}$ are shown. In both thermal cycle conditions, $\Delta\varepsilon_{cr}$ of the 1st bump (on PCB) is higher than the 2nd bump (between Si chips) and the upper part shows a greater strain accumulation than the lower part. Thus failures resulting from thermal fatigue fracture are most likely to occur in this region of the upper of the 1st bump during thermal cycle.

Moreover, in **Fig 7**, the stress in Si chips in the package at 125°C is shown. The maximum stress is 106MPa and mainly concentrated on the 1st Si chip and in the area close to bumps. Since this stress level is much less than the critical fracture stress, the fracture of Si chip is not expected during thermal cycle. However it must be noted that this analysis assumes perfect defect-free silicon and that processing related defects such as excessive chip chipping during saw singulation or excessive roughness during backgrinding may create local stress concentration points which could initiate fracture.

Thus from FEM simulations, we expect that the 3D chip stacked package is most likely to fail from solder joint fatigue in the upper part of 1st solder bump at the corner of the chip during thermal cycle.

We will analyze the reliability and failure mode of the real demonstrator and compare these FEM results.

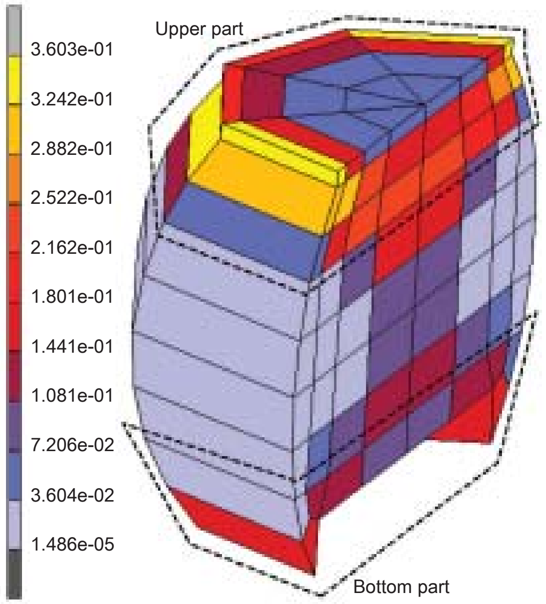

Fig. 6　Accumulated creep strain (-) in 1st bump (on PCB) in -40 to 125°C, 3cycles

Table 2　$\Delta\varepsilon_{cr}$ in the critical 1st bump (Values are averaged over the damage volumes)

Thermal cycle	1st.Bump		2nd.Bump	
	Top	Bottom	Top	Bottom
-40 to 125ºC	6.85%	4.05%	0.15%	0.19%
0 to 100ºC	4.09%	1.87%	0.05%	0.07%

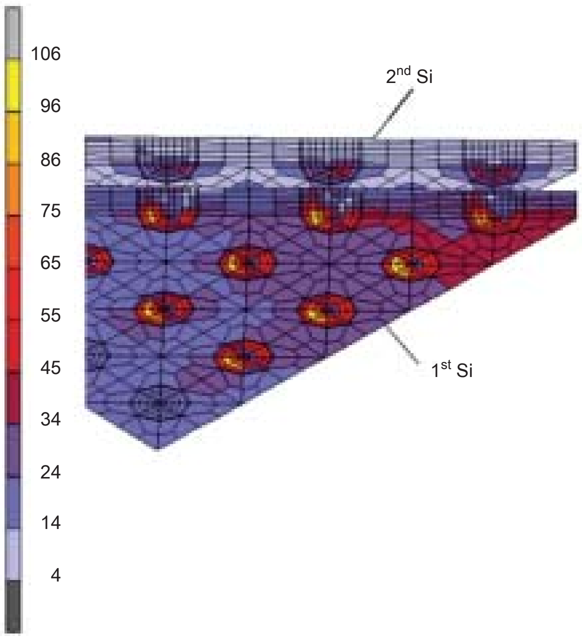

Fig. 7　Von Mises stress in Si chips at 125°C

4.2　Influence of thickness of Si chip

In a real 3D chip stacked package, Cu via holes are formed in Si chips to connect Si chips electrically. In this case, the thinner Si wafer is preferred, because it is easier to form via holes.

The behavior of the 3D chip stacked package with Si chips of different thickness by FEM simulation is analysed in this section. In this analysis, we choose thermal cycle condition -40 to 125°C and use the same FE model with **Fig. 2** with varying chip thickness.

Figure 8 shows $\Delta\varepsilon_{cr}$ in the critical 1st bump on PCB when the thickness of Si chip is changed from 50µm to 400µm. The thinner Si chips result in a lower $\Delta\varepsilon_{cr}$ in solder bumps. This is attributed to the fact that the thinner chips have less stiffness and the imposed deformation on the solder joint is thus lower.

However, the maximum creep strain in the package is still high (5.12%), so we will need to find the solution to decrease the strain in the solder joint.

On the other hand, the von Mises stress in the Si chip increases when the chip becomes thinner (**Fig. 9**). Nevertheless, the maximun stress reached is 188MPa. Therefore, the fracutre of Si chips is not expected during the thermal cycle test even if thinner Si chips are used.

4.3　Stress of Cu via hole in Si chip

During manufacturing and subsequent thermal loads, Cu via holes are subjected to thermal stresses and strains.[6] If a higher strain or stress is generated in the via hole, it would be a driving force for fatigue crack initiation and

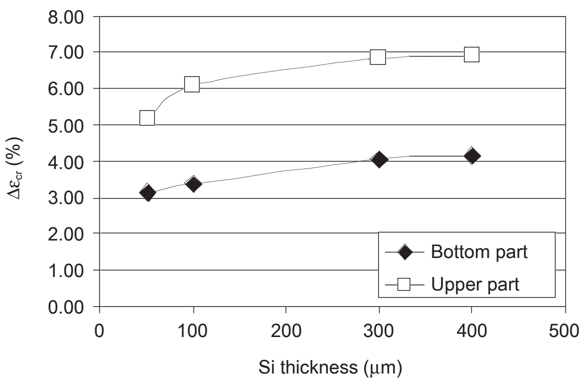

Fig. 8　$\Delta\varepsilon_{cr}$ in 3D chip stacked package for different Si chip thickness

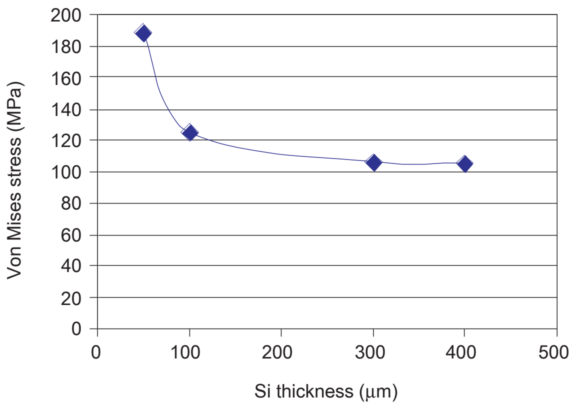

Fig. 9　Maximum von Mises stress in Si chips for different Si chip thickness

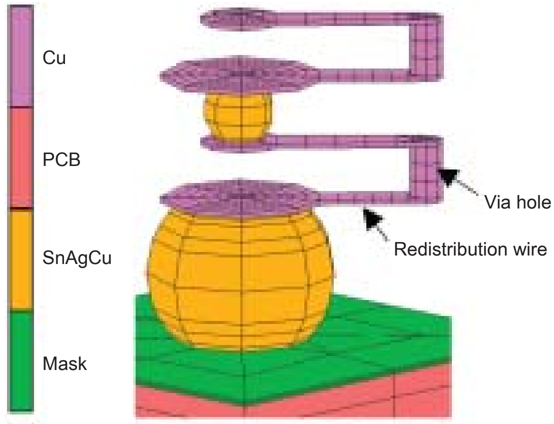

Fig. 10　FE model of 3D chip stacked package with Cu via hole and Cu redistribution path (Si and solder mask are eliminated.)

propagation to failure.

For this purpose, a FE model with Cu via holes and Cu re-distribution paths was constructed. **Figure 10** shows a partial view of this model for this. The thickness of Si chip is 100μm and the diameter of via hole is 50μm. And the diameter of Sn-Ag-Cu solder ball for 2nd bump is 130μm. Other dimensions are the same as **Fig. 2**.

Figure 11 shows the von Mises stress in the Cu via hole, re-distribution paths and pad around 1st Si chip at 125°C. The stress in Cu is the largest at 125°C during thermal cycle. From this result, the stress of Cu in via hole is less than 145MPa and problems with Cu are not expected.

We will compare this FEM simulation result with measurements of real sample in the future work.

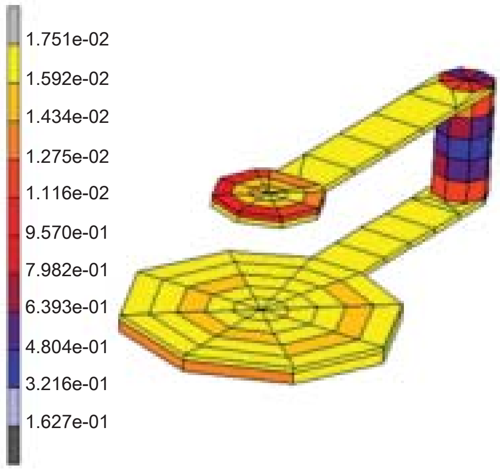

Fig. 11　Von Mises stress in Cu pad, re-distribution path and via hole at 125°C

4.4　Effect of underfill

From the results mentioned above, thin Si chip is expected to decrease the creep strain in solder bumps and improve the life-time of the 3D chip stacked package. However, the $\Delta\varepsilon_{cr}$ value is still high. An option to reduce the high strain levels is to use an underfill.

Figure 12 shows the FE model with under-fill. An underfill layer is applied in the gap between the 1st Si chip and the PCB. **Table 3** shows material properties of two types of underfill used in the simulation. In this model, the contact analysis, feature implemented in MSC.MARC software is applied. Contact (glue) mode is applied boundaries between underfill and solder mask and underfill and Si chip. The other dimensions are the same as **Fig. 10**.

Figure 13 shows $\Delta\varepsilon_{cr}$ in 1st bump and 2nd bump at corner,

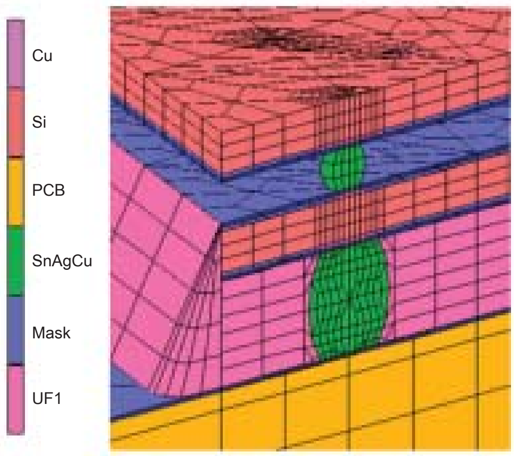

Fig. 12　FEM model of 3D chip stacked package with underfill

Table 3　Material properties of underfill

Underfill	Young's modulus (MPa)	CTE (10^{-6}/ºC)	Poisson's ratio
UF1	5000	50	0.3
UF2	10000	25	0.3

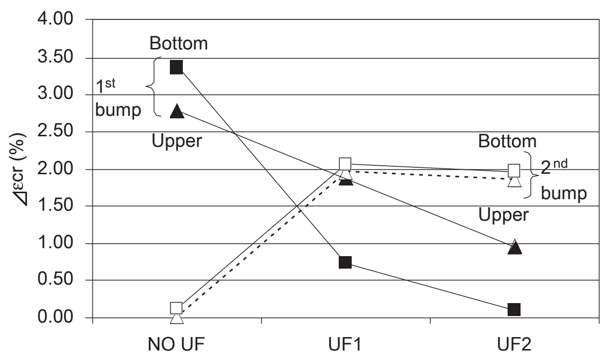

Fig. 13　$\Delta\varepsilon_{cr}$ in solder bump at corner

when the underfill is applied. From this result, as expected, $\Delta\varepsilon_{cr}$ in 1st bump is reduced due to the strain redistribution by the underfill. This reduction is higher when using UF2 since this material has a CTE closer to that of the solder is used in the package.

However, at the same time, the $\Delta\varepsilon_{cr}$ in 2nd bump increases. This behavior is observed for both underfills cases. The $\Delta\varepsilon_{cr}$ doesn't depend on the kind of underfill and is about 2% at both upper and bottom of 2nd bump.

The maximum $\Delta\varepsilon_{cr}$ in 3D chip stacked package can be reduced by using an underfill around 1st bump. However, it is expected that the failure location is shifted to the 2nd bump during thermal cycle.

5. FUTURE WORK

The simulation results will be validated by thermal cycling experiments which are on going during the writing of this paper. Their results will be shown at the conference. A second validation method is to measure the absolute stress in the silicon chip using Raman stress measurement technique.

6. CONCLUSIONS

The reliability of the 3D chip stacked package was investigated by FEM simulation. In the package, two Si chips of 300μm thickness are vertically stacked on PCB with Sn-Ag-Cu solder bumps. The FEM simulation result shows that the failure position is expected the top part of the critical solder bump joining the lower chip and the PCB during a thermal cycle test.

Furthermore, the possibility of improvement of the thermo-mechanical reliability for the package is investigated. The study shows that thinner Si chip and use of under-fill can decrease the $\Delta\varepsilon_{cr}$ in solder bumps.

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